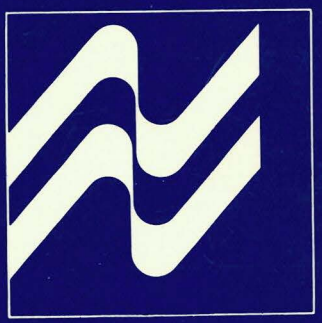
NEW DATA UPDATE 7

NATIONAL SEMICONDUCTOR CORPORATION



SEPTEMBER 1982

NEW DATA UPDATE 7

NATIONAL SEMICONDUCTOR CORPORATION

The New Data Update 7 is provided by National Semiconductor in order to keep you abreast of the latest products available. This special issue features the first pages of data sheets published April through September 1982 (2 quarters). Two alphanumerical indexes, one by device number and one by device function, serve as guides to the contents of this Update. These indexes/tables of contents are located in the front of the book, along with three other small indexes which list the new application notes, briefs, and technical papers for this quarter. One additional index serves as an ordering guide for all other application notes and briefs which are still available (this index is located in the back of the book).

Circle the appropriate update number on the business reply card (centerfold), add postage, and drop it in the mail to receive the complete data sheet of your choice. To order publications without an update number, please use the order number provided in the index and write it in one of the blanks provided on the reply card. Due to the costs of handling and mailing, we ask that you limit your requests to no more than 5 items.

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As integrated circuits become more and more complex, the benefit of consistently high quality products becomes increasingly more important to customers, many of whom have long recognized National as *the* outstanding supplier of top quality products. Such recognition is the result of a management-driven Quality Improvement Program that has pervaded every manufacturing operation, from product design through assembly and packaging at National Semiconductor Corporation. Progress has been nothing less than dramatic, and National's commitment to quality will remain unrelenting in the decades to come.

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113905	TP-18 Implementation of a Speech Synthesizer	9/82

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National Semiconductor

June 1982

ADC0820 8-Bit High Speed μP Compatible A/D Converter with Track/Hold Function

General Description

The ADC0820 is a CMOS 8-bit A/D converter which uses a half-flash technique consisting of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

This converter's input acquisition time is much faster than its conversion time and is capable of measuring many analog signals without the aid of a sample-and-hold.

This A/D is designed to appear as memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Key Specifications

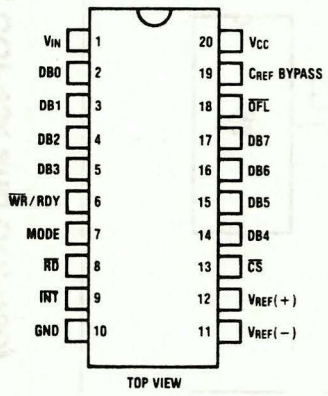
- Resolution — 8 Bits
- Conversion Time — 2.5 μs Max (RD Mode); 1.2 μs Max (WR-RD Mode)
- Input signals with slew rate of 100 mV/μs converted without external sample-and-hold to 8 bits
- Low Power — 35 mW
- Total Unadjusted Error — ± 1/2 LSB and ± 1 LSB

Features

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Easy interface to all microprocessors, or operates stand-alone
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than V_{CC}.
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Overflow output available for cascading
- 0.3" standard width 20-pin DIP

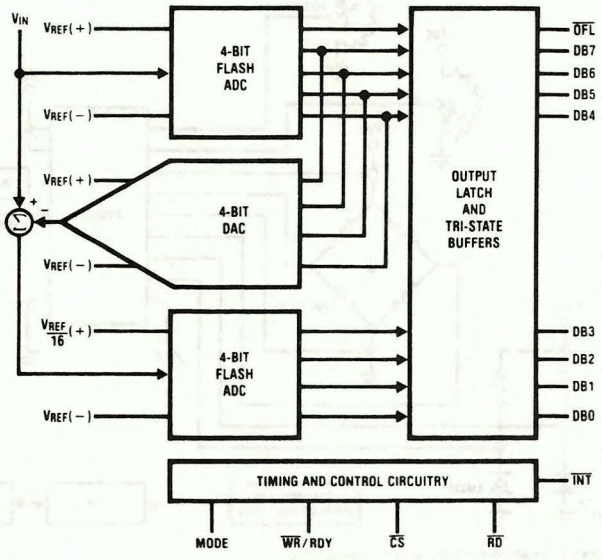
Connection Diagram

Dual-In-Line Package



TOP VIEW

Functional Diagram



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Circle DATA UPDATE No. 100584

ADC0820 8-Bit High Speed μP Compatible A/D Converter with Track/Hold Function

National Semiconductor

June 1982

ADC0831, ADC0832, ADC0834 and ADC0838 (COP431, COP432, COP434 and COP438) 8-Bit Serial I/O A/D Converters with Multiplexer Options

General Description

The ADC0831 series are 8-bit successive approximation A/D converters with a serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, and can interface with standard shift registers or μPs.

The 2-, 4- or 8-channel multiplexers are software configured for single-ended or differential inputs as well as channel assignment.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

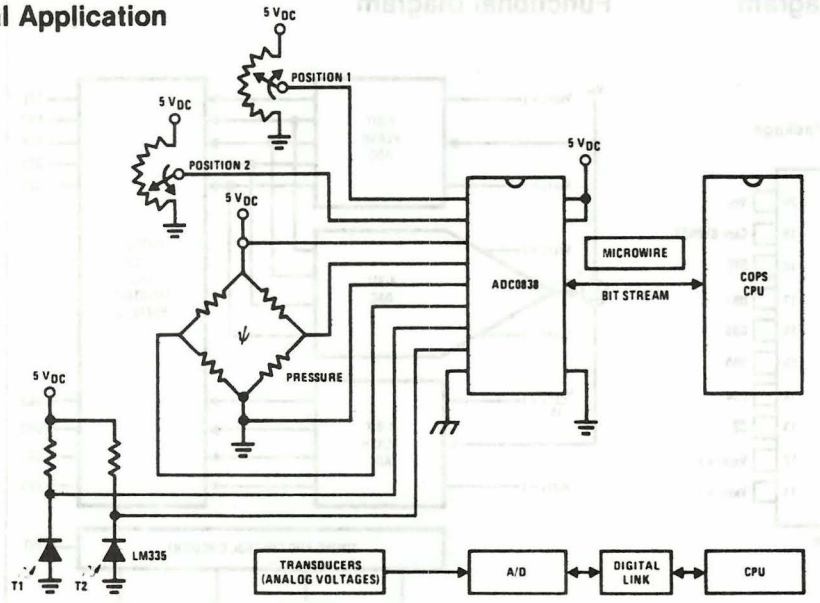
Features

- NSC MICROWIRE compatible—direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand-alone"
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 2-, 4- or 8-channel multiplexer options with address logic
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- T^2L/MOS input/output compatible
- 0.3″ standard width 8-, 14- or 20-pin DIP package

Key Specifications

Resolution	8 Bits
Total Unadjusted Error	± 1/2 LSB and ± 1 LSB
Single Supply	5 V_{DC}
Low Power	15 mW
Conversion Time	32 μs

Typical Application



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Circle DATA UPDATE No. 100593

ADC0831, ADC0832, ADC0834 and ADC0838 (COP431, COP432, COP434 and COP438) 8-Bit Serial I/O A/D Converters with Multiplexer Options

National Semiconductor

March 1982
PRELIMINARY

ADC1001, ADC1021 10-Bit μP Compatible A/D Converters

General Description

The ADC1001 and ADC1021 are CMOS, 10-bit successive approximation A/D converters. The 20-pin ADC1001 is pin compatible with the ADC0801 8-bit A/D family. The 10-bit data word is read in two 8-bit bytes, formatted left justified and high byte first. The six least significant bits of the second byte are set to zero, as is proper for a 16-bit word.

The 24-pin ADC1021 outputs 10 bits in parallel and is intended for interface to a 16-bit data bus.

A differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 10 bits of resolution.

- Easily interfaced to 6800 μP derivatives with minimal external logic
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference
- 0.3" standard width 20-pin DIP package or 24 pins with 10-bit parallel output

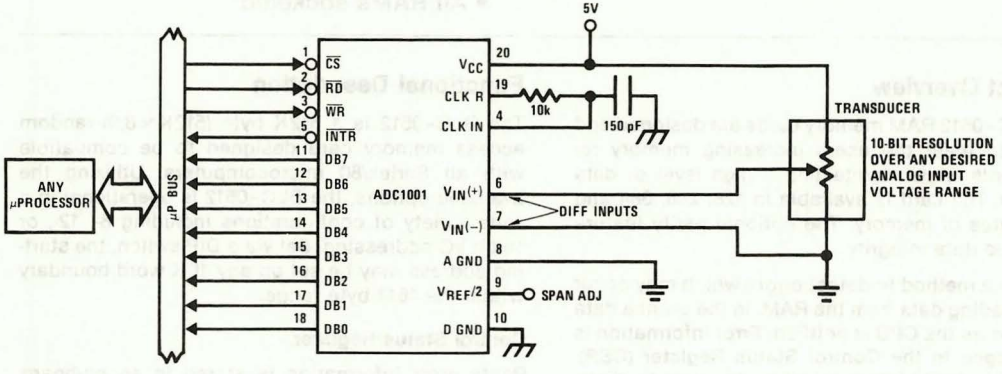
Features

- ADC1001 is pin compatible with ADC0801 series 8-bit A/D
- Compatible with NSC800 and 8080 μP derivatives — no interfacing logic needed — access time 170 ns

Key Specifications

■ Resolution	10 bits
■ Linearity error	± 1 LSB
■ Conversion time	200 μs

Typical Application



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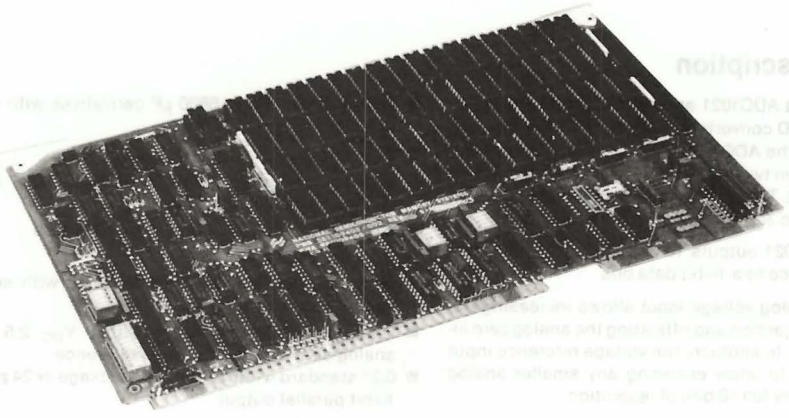
Circle DATA UPDATE No. 100600

National Semiconductor

November 1981

BLC-0512
512K-Byte Memory Card Family



- **Features**
  - Parity (error detection)
  - Selectable parity interrupt
  - 512K bytes memory
- **Enhanced Systems Performance**
  - On-board refresh and control logic
  - Internal (transparent) refresh
  - Optional external refresh
  - Battery backup capability
- **MULTIBUS™ IEEE 796 Standard**
- **Compatible with all Series/80 Boards and Card Cages**
- **Flexible Systems Capability**
  - 8- or 16-bit data bus
  - 20- or 24-bit memory addressing
  - 8-, 12-, or 16-bit I/O addressing
- **Ease of Maintenance**
  - Control status register logs failures for CPU
  - All RAMs socketed

Product Overview

The BLC-0512 RAM memory cards are designed and tested to meet the users increasing memory requirements while maintaining a high level of data integrity. The card is available in 128, 256, 384 and 512K bytes of memory. The optional parity feature enhances data integrity.

Parity is a method to detect errors which may occur while reading data from the RAM. In the event a data error occurs the CPU is notified. Error information is also logged in the Control Status Register (CSR). Selectable parity interrupts allow the user to determine which interrupt request line is used. Any one of eight interrupt request lines may be selected.

Functional Description

The BLC-0512 is a 512K byte (512K × 8,9) random access memory card designed to be compatible with all Series/80 microcomputers. Utilizing the available options, the BLC-0512 is operational in a wide variety of configurations including 8-, 12-, or 16-bit I/O addressing. Set via a DIP switch, the starting address may be set on any 16K word boundary within the 16M byte range.

Control Status Register

Parity error information is stored in an on-board CSR. The CSR is a software addressable 16-bit Control Status Register. The CSR may be set to respond

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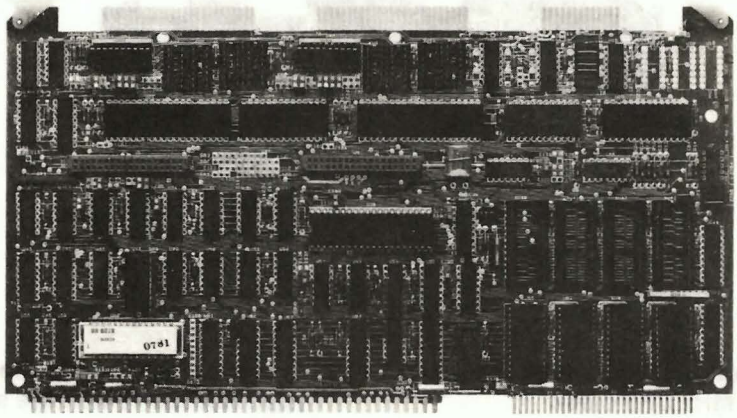
Circle DATA UPDATE No. 101527

National Semiconductor

June 1982

BLC-80/24, BLC-80/28 Board Level Computers



- **Upward compatible with BLC-80/204 Board Level Computer**
- **8085A-2 CPU operating at 4.8 or 2.4 MHz**
- **Two BLX bus connectors for BLX expansion modules**
- **4K bytes of static read/write memory with BLC-80/24, 8K bytes with BLC-80/28**
- **Sockets for up to 32K bytes of read only memory, supports 2758s, 2716s, 2732s, 2764s**
- **RAM/ROM shadowing**
- **48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators**
- **Programmable synchronous/asynchronous RS232C compatible serial interface with software selectable baud rates**
- **Full MULTIBUS™ control logic for multimaster configurations and system expansion**
- **Two programmable 16-bit BCD or binary timers/event counters**
- **12 levels of programmable interrupt control**
- **Auxiliary power bus, memory protect, and power-fail interrupt control logic provided for battery backup RAM requirements**
- **Plug-replacements for Intel SBC-80/24**

Product Overview

The National BLC-80/24 and BLC-80/28 Board Level Computers are members of National's complete line of OEM microcomputer systems which take full advantage of the latest LSI technology to provide economical, self-contained computer-based solutions for test systems, industrial control, and OEM applications. The BLC-80/24 and BLC-80/28 boards are complete computer systems on a single 6.75 x 12.00-inch printed circuit card. The CPU, system clock, BLX bus interface, read/write memory, read only memory sockets, I/O ports and drivers, serial communications interface, priority interrupt logic, and programmable timers all reside on the board. Full MULTIBUS interface logic is included to offer compatibility with the National OEM Microcomputer Systems family of Board Level Computers, expansion memory options, digital and analog I/O expansion boards, and peripheral and communications controllers.

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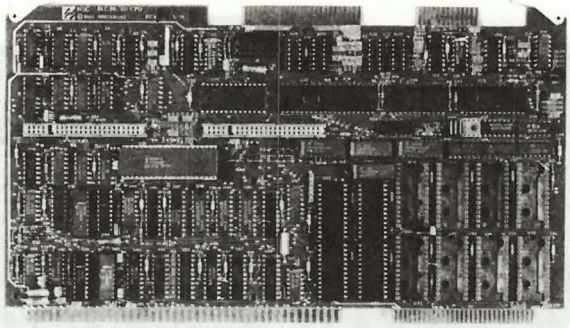
BA-B30M62/Printed in U.S.A.

Circle DATA UPDATE No. 101504

BLC-86/05
Board Level Computer



- **Designed around 8086-2 microprocessor with 5 or 8 MHz CPU clock**
- **Fully software compatible with BLC-86/12B Board Level Computer**
- **Optional numeric data processing with BLC-337 Expansion Module processor**
- **8 K bytes of static RAM**
- **Sockets for up to 64 K bytes of JEDEC 24/28-pin standard memory devices**
- **Two BLX™ bus connectors**
- **24 programmable parallel I/O lines**
- **Programmable synchronous/asynchronous RS232C compatible serial interface with software selectable baud rates**
- **Two programmable 16-bit BCD or binary timers/event counters**
- **9 Levels of vectored interrupt control, expandable to 65 levels**
- **MULTIBUS™ interface for multimaster configurations and system expansion**
- **Supported by a complete family of board level computers, memory, digital and analog I/O, peripheral controllers, packaging and software**
- **Plug replacement for Intel SBC-86/05**

Product Overview

The BLC-86/05 Board Level Computer is a member of National Semiconductor's complete line of microcomputer systems which take full advantage of the latest technology to provide economical, computer-based solutions for test systems, industrial control, and OEM applications. The BLC-86/05 board is a complete computer system on a single 6.75 × 12.00-in. printed circuit board. The CPU, system clock, read/write memory, non-volatile read only memory, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the board. The large control storage capacity makes the BLC-86/05 board ideally suited for control-oriented applications such as process control, instrumentation, industrial automation, and many others.

Functional Description

Central Processing Unit

The central processor for the BLC-86/05 board is an 8086-2 microprocessor. A clock rate of 8 MHz is supported with a jumper selectable option of 5 MHz. The CPU architecture includes four 16-bit byte addressable data registers, two 16-bit memory base pointer registers and two 16-bit index registers, all accessed by a total of 24 operand addressing modes for comprehensive memory addressing and for support of the data structures required for today's structured, high level languages, as well as assembly language.

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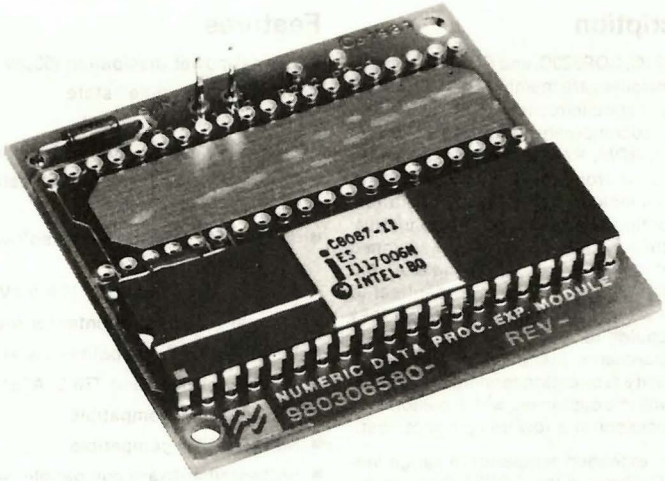
DA-B30M52/Printed in U.S.A.

Circle DATA UPDATE No. 101525

National Semiconductor

June 1982

BLC-337
Numeric Data Processor Expansion Module



- **Fast fixed and floating point functions for BLC-86/12B and BLC-86/05**
- **Contains the powerful 8087 numeric data processor**
- **Supports single and double precision integer, floating point and others, for a total of seven data types**
- **Plug replacement for Intel SBC-337**
- **Magnifies host CPU instruction set with arithmetic, logarithmic, transcendental, and trigonometric instructions**
- **Proposed IEEE floating point standard is used for high accuracy**
- **Easy to install, plugs into CPU socket on host board**

Product Overview

The BLC-337 is a member of National's growing line of Series/80 Board Level Expansion Modules. High performance numerics support for 8086-based CPU boards such as the BLC-86/12B single board computer user is available for simulation, instrument automation, graphics, signal processing, and business systems. Expanding the instruction set with greater than 60 numeric instructions supporting six data types is provided by coprocessor interface between the 8087 and the CPU. To install the BLC-337, one simply removes the host CPU chip from its socket, plugs the BLC-337 into the host board's CPU socket, and reinstalls the CPU chip into the socket provided on the BLC-337.

Functional Description

The Numeric Data Processor (NDP) is internally divided into two processing elements: the control unit (CU) and the numeric execution unit (NEU), which provides for concurrent operation of the two units. The NEU executes all numeric instructions, while the CU receives and decodes instructions, reads and writes memory operands and executes processor control instructions.

Control Unit

The CU keeps the 8087 operating in synchronization with its host CPU. 8087 instructions are intermixed with CPU instructions in a single instruction stream. The CPU fetches all instructions from memory; by monitoring the status signals emitted by the CPU, the NDP control unit determines when an 8086 instruc-

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DA-B30M52/Printed in U.S.A.

Circle DATA UPDATE No. 101290

National Semiconductor

July 1982

COP420C/COP421C and COP320C/COP321C Single-Chip CMOS Microcontrollers

General Description

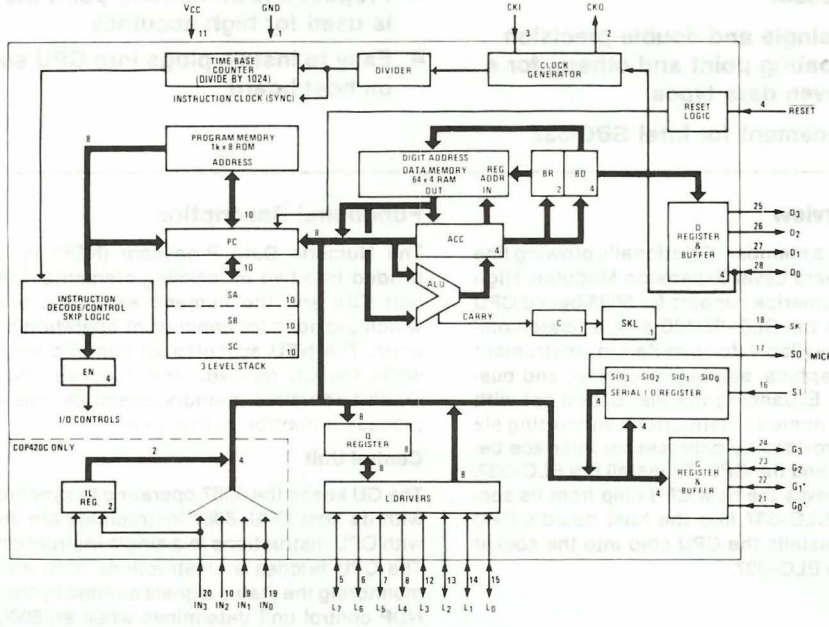
The COP420C, COP421C, COP320C, and COP321C Single-Chip CMOS Microcontrollers are members of the COPS™ family, fabricated using complementary MOS technology. They are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD and binary data manipulation. The COP421C is identical to the COP420C, except with 19 I/O lines instead of 23. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Control Oriented Processor at a low end-product cost.

The COP320C is the extended temperature range version of the COP420C (likewise the COP321C is the extended temperature range version of the COP421C). The COP320C/321C are exact functional equivalents of the COP420C/421C.

Features

- Lowest power dissipation (50 μW typical)
- Power saving "Idle" state
- Powerful instruction set
- 1k × 8 ROM, 64 × 4 RAM, 23 I/O lines (COP420C)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- 15 μs instruction time, plus software selectable oscillators
- Single supply operation (2.4-5.5V)
- Internal time-base counter for real-time processing
- MICROWIRE™ compatible serial I/O
- General purpose and TRI-STATE® outputs
- LSTTL/CMOS compatible
- MICROBUS™ compatible
- Software/hardware compatible with other members of COP400 family
- Extended temperature range device COP320C/COP321C (−40°C to +85°C)

COP420C/421C and COP320C/321C Block Diagram



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Circle DATA UPDATE No. 101984

COP420C/COP421C and COP320C/COP321C
Single-Chip CMOS Microcontrollers

National Semiconductor

MARCH 1982

COP420R/COP444LR Piggyback-EPROM Microcontroller

General Description

The COP420R and COP444LR Piggyback-EPROM microcontrollers are members of the COPS™ family. The COP420R and COP444LR devices are identical to the COP420 and COP444L respectively except that the program ROM has been removed. In place of the ROM each device package incorporates the circuitry and socket to accommodate the Piggyback-EPROM.

The socket provided on the package accepts an MM2716, NMC27C16, MM2758A, or MM2758B EPROM. Each part is a complete microcontroller system with CPU, RAM, I/O, and EPROM socket provided in a single 28-pin package. In a system the COP420R and COP444LR will perform exactly as its mask programmed equivalent.

The complete package allows field test of a system in its final electrical and mechanical configuration. This important benefit facilitates development and debug of a COP400 program prior to masking of a production part.

These devices are also economical in low and medium volume applications or when the program may require changing.

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Features

- Exact equivalent of the COP420 and COP444L — plugs into same socket
- Socket and interface for industry standard EPROMs
- Self-contained voltage regulator for EPROM on COP444LR
- Powerful instruction set
- True vectored interrupt, plus restart
- Three-level subroutine stack
- Compatible with all COPS family peripherals
- Internal binary counter register with MICROWIRE™ family peripherals compatible serial I/O
- Software and hardware compatible with other members of the COPS family
- Single supply operation
- Internal presettable time base counter for real time processing
- 4 μs instruction time (COP420R)
- 16 μs instruction time (COP444LR)
- 23 I/O lines

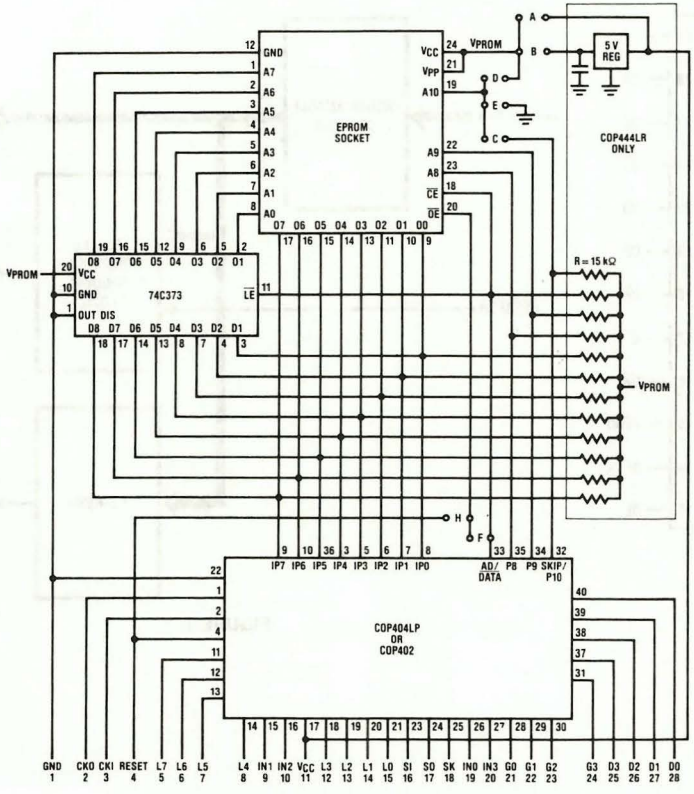
EPROM SOCKET
COP444LR ONLY
5 V REG
74C373
R = 15 kΩ
VPROM
COP404LP OR COP402
GND CKO CKI RESET L7 L6 L5 L4 IN1 IN2 VCC L3 L2 L1 L0 SI SO SK IN0 IN3 G0 G1 G2 G3 D3 D2 D1 D0

Figure 1. COP420R/COP444LR Block Diagram

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Circle DATA UPDATE No. 101986

National Semiconductor

PRELIMINARY
August 1982

DP84300 Programmable Refresh Timer

General Description

The DP84300 programmable refresh timer is a logic device which produces the desired refresh clock required by all dynamic memory systems.

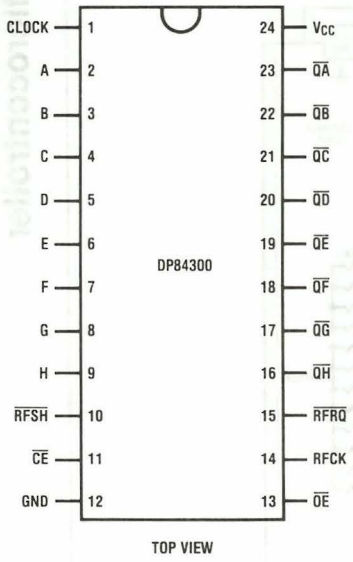
Additional circuitry has been included in the device to minimize logic required by memory systems to perform refresh control.

Features

- One chip solution to produce RFCK timing for the DP8408 and DP8409 dynamic RAM controllers
- Programmable refresh clock timer allows for a maximum refresh period with most system clocks
- Timing is completely synchronous with the input clock, preventing race conditions in some memory controllers
- Includes a refresh request output, simplifying the design of refresh logic in discrete controllers

Connection Diagram

Dual-In-Line Package



TOP VIEW

Block Diagram

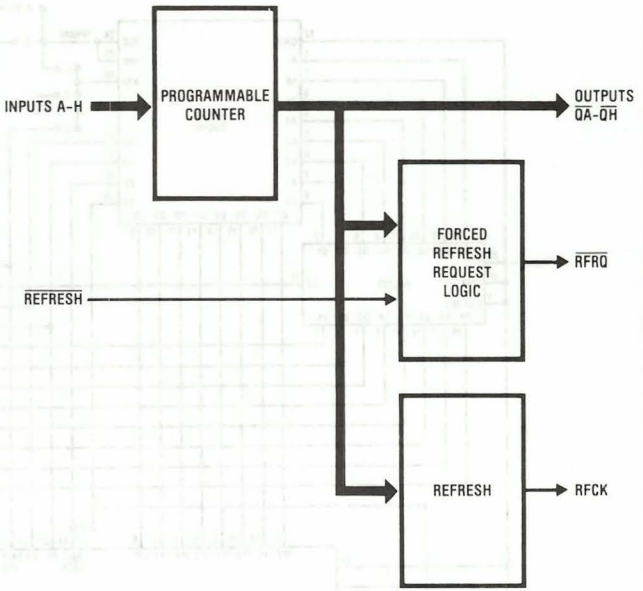


FIGURE 1

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Circle DATA UPDATE No. 103078

National Semiconductor

PRELIMINARY
July 1982

DP84312 Dynamic RAM Controller Interface Circuit for the NS16032 CPU

General Description

The DP84312 dynamic RAM controller interface is a logic device which allows for easy interface between the DP8409 dynamic RAM Controller and the NS16032 microprocessor.

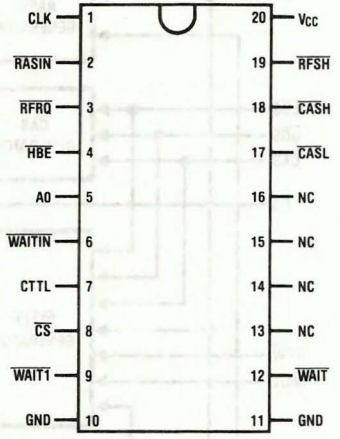
Using timing signals from the NS16201 timing and control unit and the NS16032, the DP84312 supplies all control signals needed to perform memory read, write, byte write, and refresh.

Features

- Low parts count memory system
- Allows the DP8409 to perform hidden refresh
- Allows for the insertion of wait states for slow dynamic RAMs
- Supplies independent $\overline{\text{CAS}}$s for byte writing
- 20-pin 0.3 inch wide package

Connection Diagram

Dual-In-Line Package



TOP VIEW

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Circle DATA UPDATE No. 103080

National Semiconductor

PRELIMINARY
August 1982

DP84322 Dynamic RAM Controller Interface Circuit for the 68000 CPU

DP84322 Dynamic RAM Controller Interface Circuit for the 68000 CPU

General Description

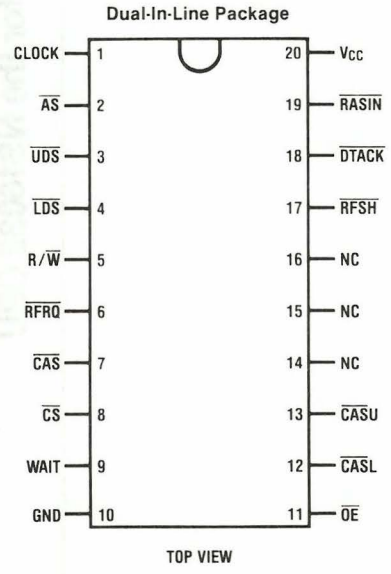
The DP84322 dynamic RAM controller interface is a logic device which allows for easy interface between the DP8409 dynamic RAM controller and the 68000 microprocessor.

The DP84322 supplies all the control signals needed to perform memory read, write and refresh. Logic is included for inserting a wait state when using fast CPUs.

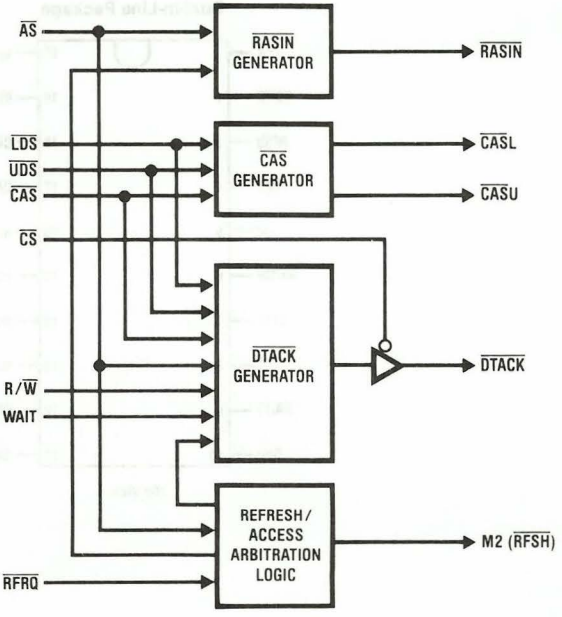
Features

- Provides 3-chip solution for the 68000 CPU and dynamic RAM interface
- Works with all 68000 speed versions
- Performs hidden refresh
- $\overline{\text{DTACK}}$ is automatically inserted for both memory access and memory refresh
- Performs forced refresh using typically 4 CPU clocks

Connection Diagram



Block Diagram



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Circle DATA UPDATE No. 103085

National Semiconductor

PRELIMINARY
July 1982

DP84332 Dynamic RAM Controller Interface Circuit for the 8086 and 8088 CPUs

DP84332 Dynamic RAM Controller Interface Circuit for the 8086 and 8088 CPUs

General Description

The DP84332 dynamic RAM controller interface is a logic device which allows for easy interface between the DP8408 dynamic RAM controller and the 8086 and 8088 microprocessors. No wait states are required for memory access, even for the 10 MHz microprocessors. Memory refreshing may be hidden (no wait states) or forced (up to three wait states).

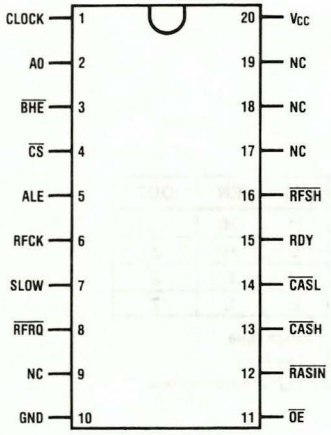
The DP84332 supplies all the control signals needed to perform memory read, write, and refresh. Logic is also included to insert a wait state when using slow memory.

Features

- Low parts count controller for the DP8408/DP8409
- Works with 8086 systems configured in min or max mode
- Performs hidden refresh using the DP8408 dynamic RAM controller
- Compatible with both the 8086 and 8088 microprocessors
- Capable of working at all CPU clock frequencies up to 10 MHz

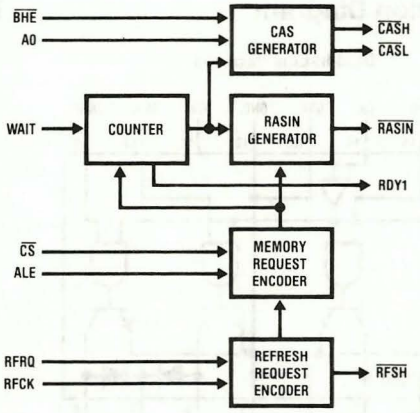
Connection Diagram

Dual-In-Line Package



TOP VIEW

Block Diagram



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Circle DATA UPDATE No. 103093

National Semiconductor

PRELIMINARY
April 1982

DS3658 Quad High Current Peripheral Driver

General Description

The DS3658 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. A unique input circuit combines TTL compatibility with high impedance. In fact, its extreme low input current allows it to be driven directly by a CMOS device. Output clamp diodes are provided for protection when driving inductive loads. An on-chip protection circuit guarantees glitch-free operation during power up or down, and a fail safe feature is provided which puts the output in high impedance state when the input is open.

Applications

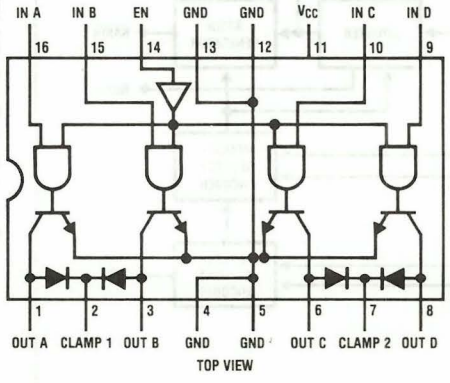
- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Single saturated transistor outputs
- Low standby power, 10 mW typical
- High impedance TTL compatible inputs
- Outputs may be tied together for increased current capacity
- High output current
  - 600 mA per output
  - 2.4A per package
- No output latch-up at 35V
- Low output ON voltage (350 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

Connection Diagram

Dual-In-Line Package



TOP VIEW

Truth Table

IN	EN	OUT
H	H	L
L	H	Z
H	L	Z
L	L	Z

H = High state
L = Low state
Z = High impedance state

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Circle DATA UPDATE No. 103325

National Semiconductor

April 1982

DS3680 Quad Negative Voltage Relay Driver

General Description

The DS3680 is a quad high voltage negative relay driver designed to operate over wide ranges of supply voltage, common-mode voltage, and ambient temperature, with 50 mA sink-capability. These drivers are intended for switching the ground end of loads which are directly connected to the negative supply, such as in telephone relay systems.

Since there may be considerable noise and IR drop between logic ground and negative supply ground in many applications, these drivers are designed to operate with a high common-mode range (±20V referenced to negative supply ground). Each driver has a common-mode range separate from the other drivers in the package, which permits input signals from more than one element of the system.

With low differential input current requirements (typically 100 μA), these drivers are compatible with TTL, LS and CMOS logic. Differential inputs permit either inverting or non-inverting operation.

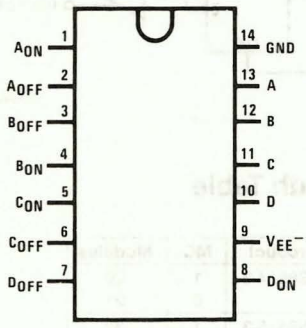
The driver outputs incorporate transient suppression clamp networks, which eliminate the need for external networks when used in applications of switching inductive loads. A fail-safe feature is incorporated to insure that, if the V_{ON} input or both inputs are open, the driver will be OFF.

Features

- −10V to −60V operation
- Quad 50 mA sink capability
- TTL/LS/CMOS or voltage comparator input
- High input common-mode voltage range
- Very low input current
- Fail-safe disconnect feature
- Built-in output clamp diode

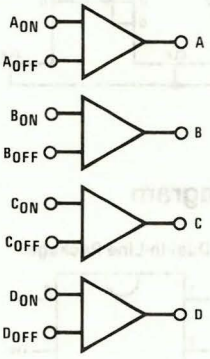
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Diagram



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Circle DATA UPDATE No. 103345

National Semiconductor

PRELIMINARY
August 1982

DS8614-3, DS8615-3, DS8616-3, DS8617-3
130 MHz Low Power Dual Modulus Prescalers

DS8614-3, DS8615-3, DS8616-3, DS8617-3 130 MHz Low Power Dual Modulus Prescalers

General Description

The DS8614-3 series products are low power dual modulus prescalers which divide by 20/21, 32/33, 40/41, and 64/65, respectively. The modulus control (MC) input selects division by N when at a high TTL level and division by N + 1 when at a low TTL level. The clock inputs are buffered, providing 40 mVrms input sensitivity. The two outputs provide the user the option to wire either a totem-pole or open-collector output structure. Additionally, the user can wire a resistor between the two output pins to minimize edge transition emissions. The outputs are designed to drive positive edge triggered PLLs. These products operate from a regulated 5V ± 10% source. Regulated operation is obtained by connecting both V_S and V_{REG} to the supply source.

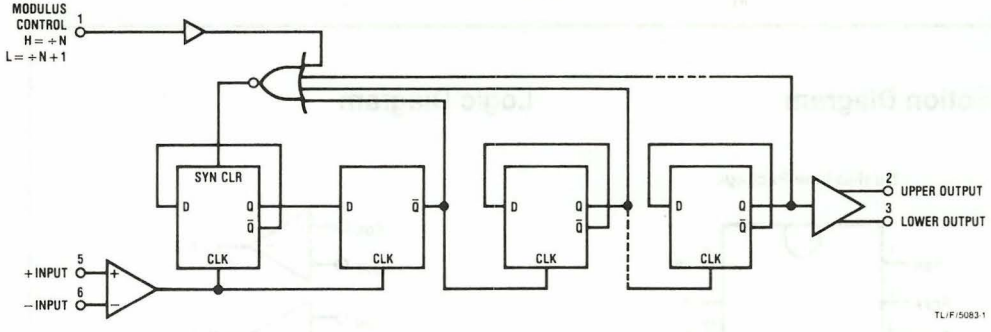
The devices can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 130 MHz.

Features

- Low power, 7 mA max
- 130 MHz toggle frequency
- 40 mVrms input sensitivity

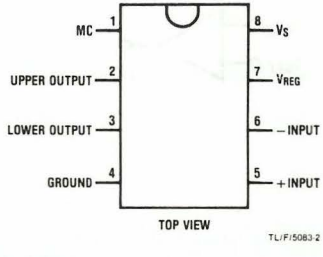
Logic Diagram

Generalized ÷ N/N + 1



Connection Diagram

Dual-In-Line Package



Truth Table

Product	MC	Modulus
DS8614-3	1	20
	0	21
DS8615-3	1	32
	0	33
DS8616-3	1	40
	0	41
DS8617-3	1	64
	0	65

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Circle DATA UPDATE No. 103349

National Semiconductor

PRELIMINARY
April 1982

DS8621 VHF/UHF Prescaler

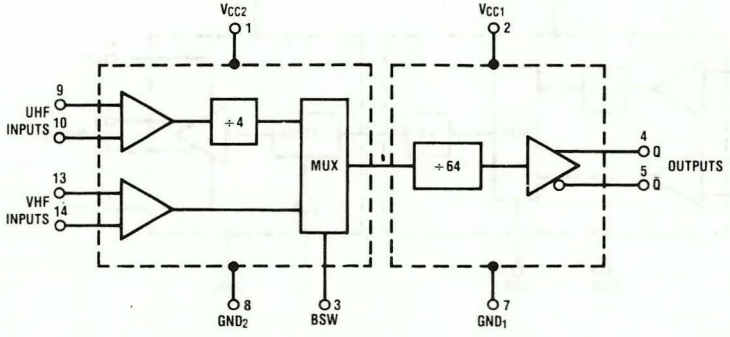
General Description

The DS8621 is a low power, high speed prescaler intended for use in frequency synthesized television tuners. The device performs division by 64 from the VHF input and division by 256 from the UHF input. The VHF and UHF inputs are buffered providing 50 mVrms sensitivity at frequencies in excess of 275 MHz and 1.2 GHz respectively. (The VHF and UHF input signals can be applied either single or double-ended.) The TTL compatible bandswitch (BSW) input selects the VHF inputs when at a low level and the UHF inputs when at a high level. The outputs are complementary ECL structures which have controlled edge-transition rates to minimize spurious harmonic emissions. The device operates from a 5V ± 10% supply source. V_{CC2} and GND_2 power the VHF and UHF input stages while V_{CC1} and GND_1 power the remainder of the circuit, thus limiting internal feedback.

Features

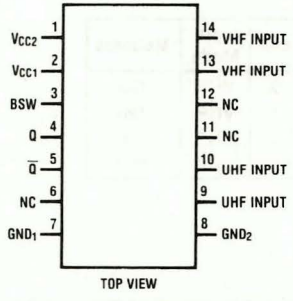
- Broadband operation
- High sensitivity
- Separate VHF and UHF inputs
- Low power
- Pin compatible with RCA (CA3179) and Motorola (MC12071)

Logic Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Truth Table

BSW	Input Mode	Modulus
0	VHF	64
1	UHF	256

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Circle DATA UPDATE No. 103355

National Semiconductor

PRELIMINARY
April 1982

DS8622 Dual Modulus VHF/UHF Prescaler

DS8622 Dual Modulus VHF/UHF Prescaler

General Description

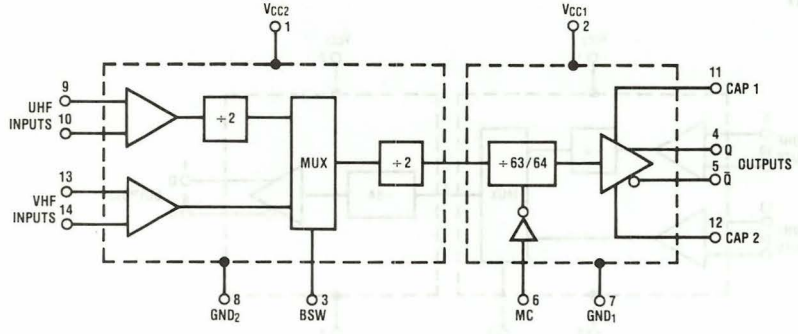
The DS8622 is a low power broadband dual modulus prescaler intended for use in frequency synthesized television tuners. The device features separate VHF and UHF buffered inputs, VHF input division by 126 or 128, UHF input division by 252 or 256, TTL compatible bandswitch and modulus control inputs, complementary ECL outputs, and 5V operation.

The VHF and UHF inputs cover a frequency range from 80 MHz to 1200 MHz and can be driven either single or double-ended. The bandswitch (BSW) input selects the VHF inputs when at a low level and the UHF inputs when at a high level. The modulus control (MC) input selects division by 126 or 252 when at a high level and division by 128 or 256 when at a low level. The dual modulus feature of this prescaler can provide frequency resolution steps of 3.9 kHz, 7.8 kHz, or 15.6 kHz as shown in the table of Possible Operating Conditions. The outputs are internally edge-transition controlled to minimize spurious harmonic emissions. CAP 1 and CAP 2 pins can also be used to further slow the edge transition times. The device operates from a standard 5V ± 10% supply source. V_{CC2} and GND_2 power the VHF and UHF input stages, and V_{CC1} and GND_1 power the remainder of the circuit, thus limiting internal feedback.

Features

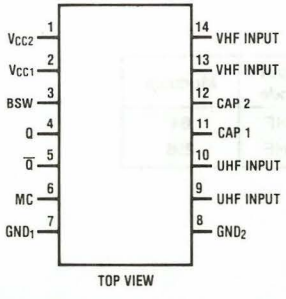
- Broadband operation
- Increased frequency resolution
- High input sensitivity
- Separate VHF and UHF inputs
- Low power

Logic Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Truth Table

BSW	MC	Input Mode	Modulus
0	0	VHF	128
0	1	VHF	126
1	0	UHF	256
1	1	UHF	252

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Circle DATA UPDATE No. 103356

National Semiconductor

PRELIMINARY
May 1982

DS8627, DS8628 225 MHz Low Power Prescalers

DS8627, DS8628 225 MHz Low Power Prescalers

General Description

The DS8627 and DS8628 are low power fixed ratio prescalers which divide by 24 and 20, respectively. The inputs can be driven either single or double ended and they are buffered, providing 40 mVrms input sensitivity. The output provided is open-collector and is capable of interfacing with TTL and CMOS.

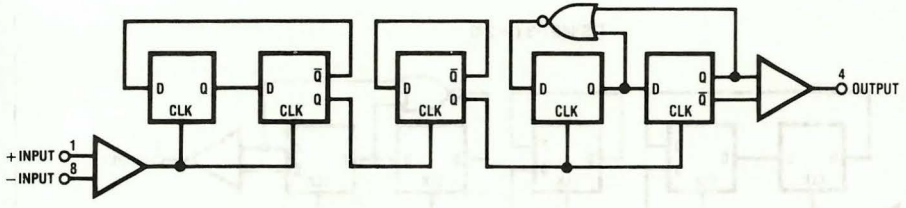
The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 225 MHz.

Features

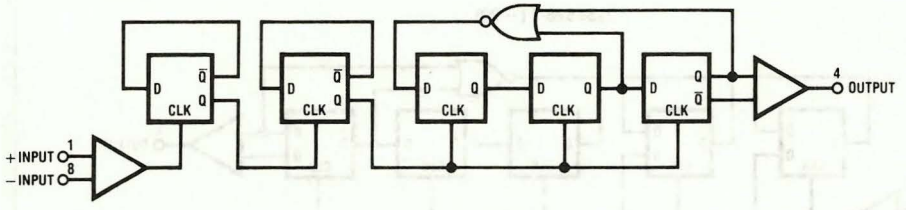
- Low power, 7 mA max
- 225 MHz toggle frequency
- 40 mVrms input sensitivity
- Pin compatible with SP8656, SP8658 prescalers

Logic Diagrams

DS8627 (÷ 24)

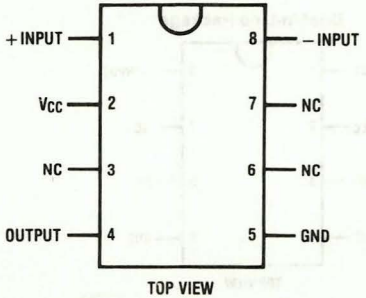


DS8628 (÷ 20)



Connection Diagram

Dual-In-Line Package



TOP VIEW

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IM-B25M52/Printed in U.S.A.

Circle DATA UPDATE No. 103361

National Semiconductor

PRELIMINARY
August 1982

DS8627-3, DS8628-3 130 MHz Low Power Prescalers

General Description

The DS8627-3 and DS8628-3 are low power fixed ratio prescalers which divide by 24 and 20, respectively. The inputs can be driven either single or double ended and they are buffered, providing 40 mVrms input sensitivity. The output provided is open-collector and is capable of interfacing with TTL and CMOS.

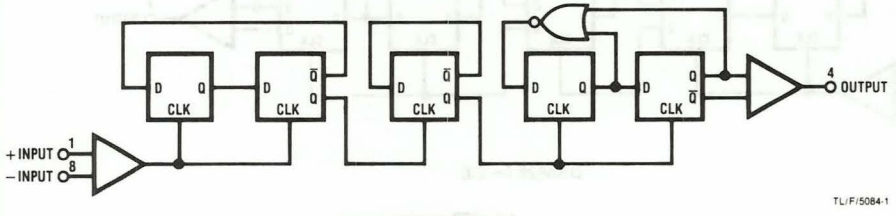
The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 130 MHz.

Features

- Low power, 7 mA max
- 130 MHz toggle frequency
- 40 mVrms input sensitivity

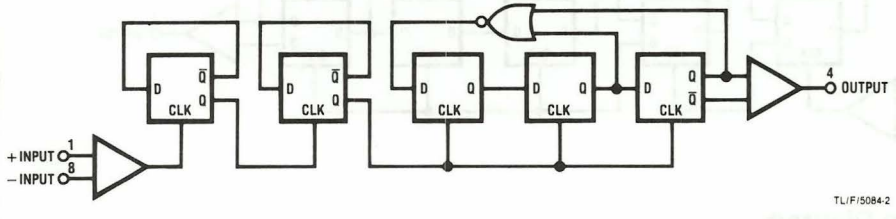
Logic Diagrams

DS8627-3 (÷ 24)



TL/F/5084-1

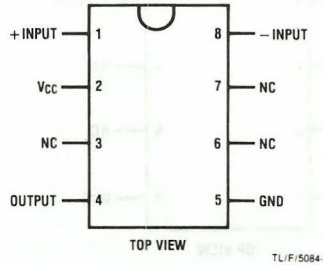
DS8628-3 (÷ 20)



TL/F/5084-2

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5084-3

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Circle DATA UPDATE No. 103362

National Semiconductor

August 1981

DT1056/DT1057 DIGITALKER™ Standard Vocabulary Kit

General Description

The DIGITALKER™ is a speech synthesis system consisting of several N-channel MOS integrated circuits. It contains a speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

The DT1056/DT1057 is a standard DIGITALKER kit encoded with 131 separate and useful words (see the Master Word List Table I) and when used with the DT1050 Standard Vocabulary Kit, provides a library of 274 useful words. The words have been assigned discrete addresses, making it possible to output single words or words concatenated into phrases or even sentences.

The "voice" output of the DT1056/DT1057 is a highly intelligible male voice. The vocabulary is chosen so that it is applicable to many products and markets.

Features

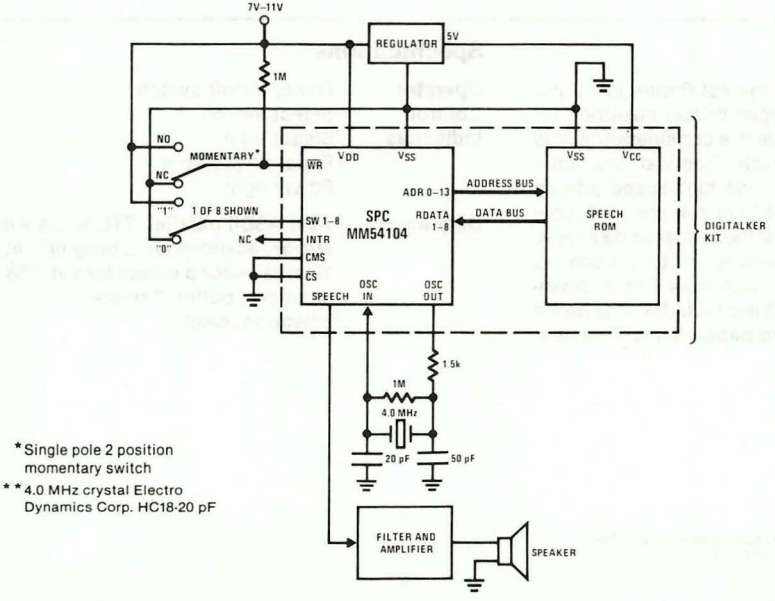
- Easily adaptable to DT1050 Standard Vocabulary Kit
- 131 useful words
- COPS™ and MICROBUS™ compatible
- Designed to be easily interfaced to other popular microprocessors
- Natural inflection and emphasis of original speech
- Addresses 128k bits of ROM directly
- TTL compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator
- Available in complete kit (DT1056) or speech ROMs only (DT1057)

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

Typical Applications

Minimum Configuration Using Switch Interface



*Single pole 2 position momentary switch

**4.0 MHz crystal Electro Dynamics Corp. HC18-20 pF

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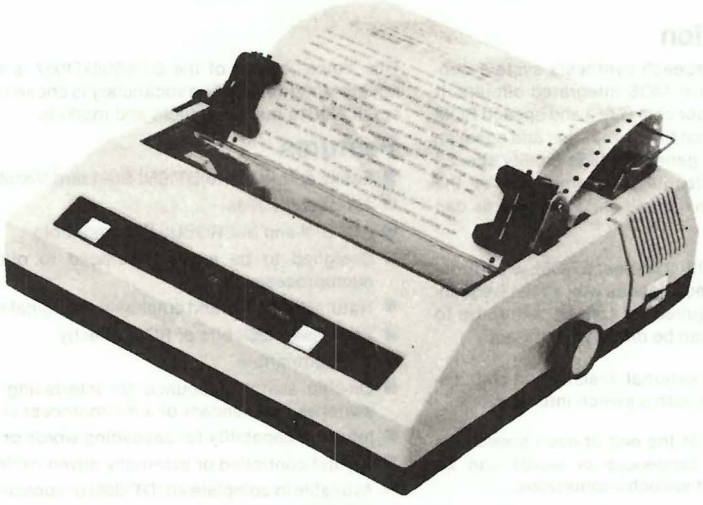
IM-B25M81/Printed in U.S.A.

Circle DATA UPDATE No. 104261

National Semiconductor

July 1982

Impact Printer



- **Compatible with STARPLEX™ and STARPLEX II™ Development Systems**
- **Compatible with 6600 series industrial microcomputer systems**
- **150 CPS at 10 CPI**
- **100% duty cycle**
- **9 × 7 dot matrix**
- **Bidirectional, logic seeking**
- **Uses standard cut-sheet, fan-fold paper**
- **40, 80, and 132 column format**
- **Light, compact, rugged**

Product Overview

The Centronics® Model 150 Impact Printer is a light, compact, versatile, and rugged printer designed for most applications where size is a consideration. It is capable of 100% duty cycle applications, thus making it a highly efficient and high-speed printer. Its snap-on tractors, top-of-form feature, and condensed print capability allow the printer to be able to print out a variety of computer output such as computer program listings, business forms, financial data and labels. The printer includes a cassette ribbon system, self-test, and paper-empty detection for operator convenience.

Specifications

Operator Control/ Indicators	Power on/off switch Select switch Select light Paper empty light Power light
Data Input	7-Bit ASCII parallel, TTL levels with strobe, acknowledge, busy 8th bit selects second character set. 768 character buffer. Remote select/deselect.

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DA-B30M72/Printed in U.S.A.

Circle DATA UPDATE No. 610400

National Semiconductor

August 1982

INS1771-1 Floppy Disk Formatter/Controller

INS1771-1 Floppy Disk Formatter/Controller

General Description

The INS1771-1 is a programmable floppy disk formatter/controller chip contained in a standard 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technolgy, interfaces a floppy disk drive directly to a computer interface bus. The INS1771-1 provides soft sector formatting, which may be either IBM 3740 compatible or a user-selected sector format.

The INS1771-1 is designed to operate on a multiplexed, TRI-STATE® 8-bit bidirectional bus with other bus-oriented devices. The chip is programmed by the system software via the bus and all data, status information, and control words are transferred over the bus lines.

Features

- Soft sector format compatibility
- Automatic track seek with verification
- Provisions for miniature floppy disk interface
- Read mode capabilities
  - — Single/multiple record read with automatic sector search or entire track read
  - — Selectable 128-byte or variable record length
- Write mode capabilities
  - — Single/multiple record write with automatic sector search
  - — Entire track write for diskette initialization
- Programmable controls
  - — Selectable track-to-track stepping time
  - — Selectable head settling and head engage times
  - — Selectable three-phase or step and direction and head positioning motor controls
- Double buffering of data
- TTL compatible
- DMA or programmed data transfers
- Reduces system component count
- On-chip CRC generation and checking
- Direct plug-in replacement for western digital FD1771

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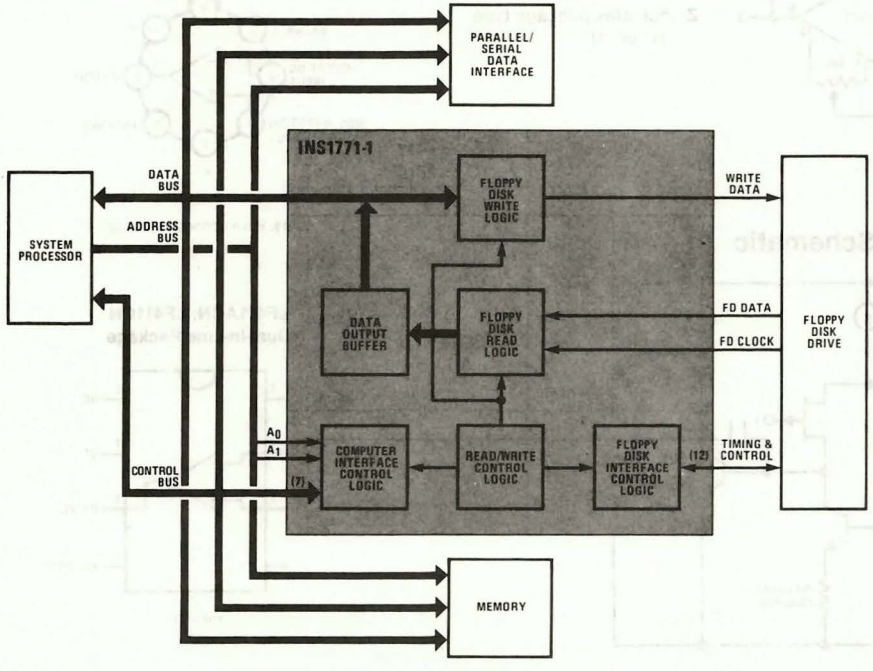

INS1771-1 General System Configuration

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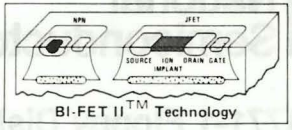
Circle DATA UPDATE No. 104900

National Semiconductor

March 1982



LF411A/LF411 Low Offset, Low Drift JFET Input Operational Amplifier

General Description

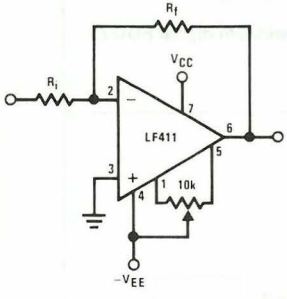
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	0.5 mV (max)
■ Input offset voltage drift	10 μV/°C (max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	3 MHz (min)
■ High slew rate	10V/μs (min)
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz	< 0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



Ordering Information

LF411XYZ

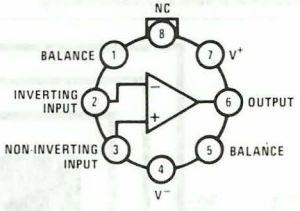
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

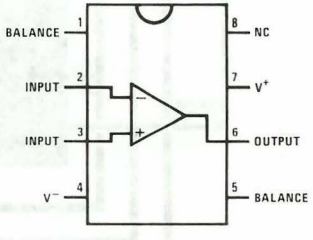
LF411AMH/LF411MH, LF411ACH/LF411CH
Metal Can Package



TOP VIEW

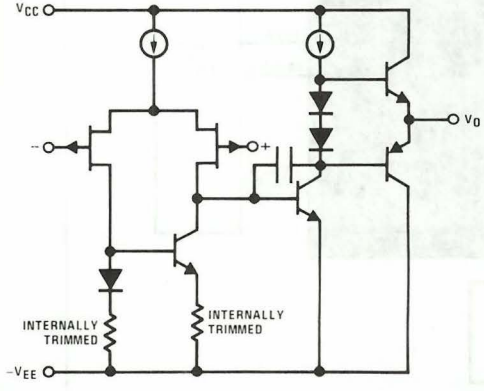
Note. Pin 4 connected to case.

LF411ACN, LF411CN
Dual-In-Line Package



TOP VIEW

Simplified Schematic



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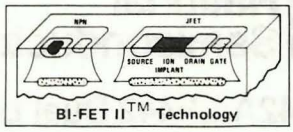
IM-B20M32/Printed in U.S.A.

Circle DATA UPDATE No. 106148

National Semiconductor

March 1982



BI-FET II™ Technology

LF412A/LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

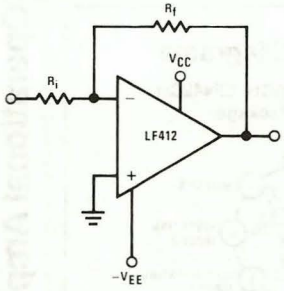
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	1 mV (max)
■ Input offset voltage drift	10 μV/°C (max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	3 MHz (min)
■ High slew rate	10V/μs (min)
■ Low supply current	1.8 mA/Amplifier
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz-20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



Ordering Information

LF412XYZ

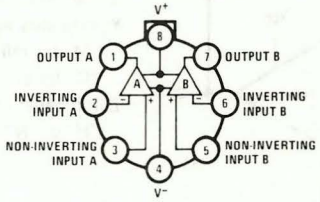
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

LF412AMH/LF412MH, LF412ACH/LF412CH
Metal Can Package

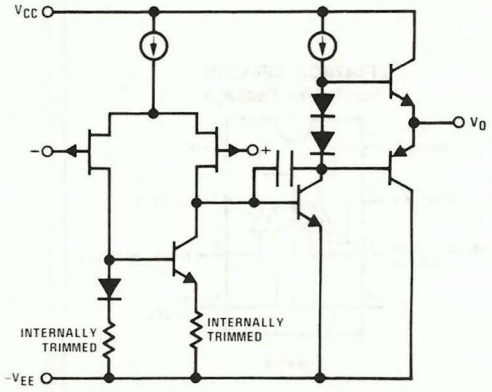


Note. Pin 4 connected to case.

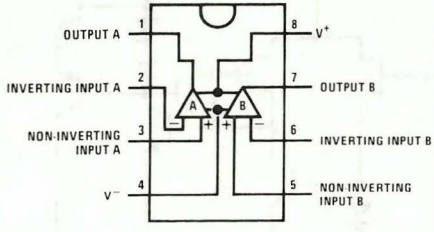
TOP VIEW

Simplified Schematic

1/2 Dual



LF412ACN, LF412CN
Dual-In-Line Package



TOP VIEW

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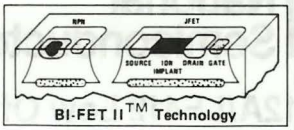
Circle DATA UPDATE No. 106149

National Semiconductor

March 1982



LF442A/LF442 Dual Low Power JFET Input Operational Amplifier

General Description

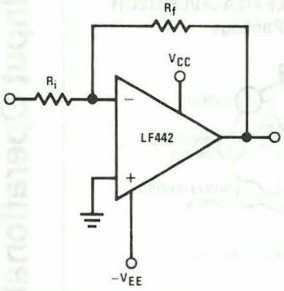
The LF442 dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

■ 1/10 supply current of a LM1458	400 μA (max)
■ Low input bias current	50 pA (max)
■ Low input offset voltage	1 mV (max)
■ Low input offset voltage drift	10 μV/°C (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Typical Connection



Ordering Information

LF442XYZ

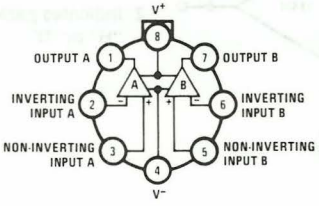
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

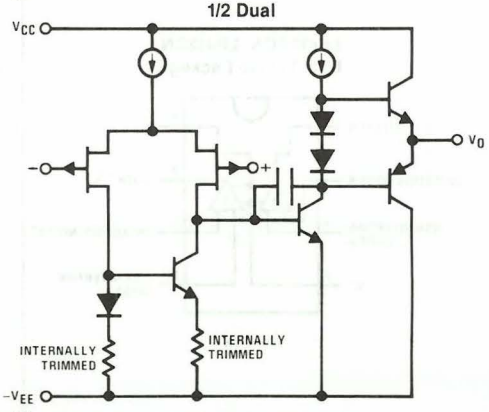
LF442AMH, LF442ACH, LF442CH
Metal Can Package



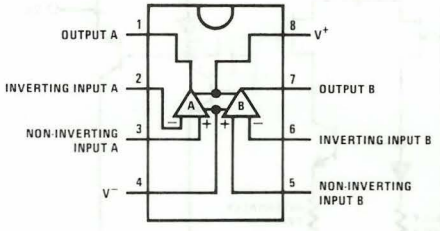
TOP VIEW

Note. Pin 4 connected to case.

Simplified Schematic



LF442ACN, LF442CN
Dual-In-Line Package



TOP VIEW

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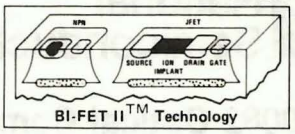
IM-B20M32/Printed in U.S.A.

Circle DATA UPDATE No. 106157

National Semiconductor

March 1982



BI-FET II™ Technology

LF444A/LF444 Quad Low Power JFET Input Operational Amplifier

General Description

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

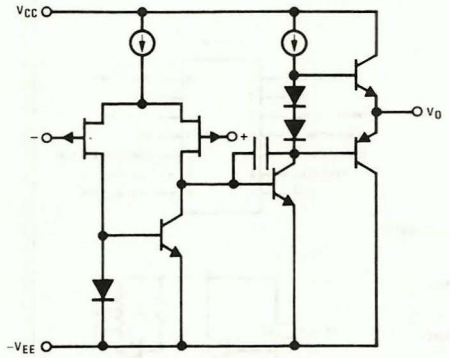
The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Features

■ 1/4 supply current of a LM148	200 μA/Amplifier (max)
■ Low input bias current	50 pA (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

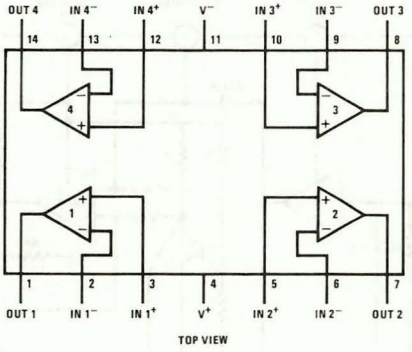
Simplified Schematic

1/4 Quad



Connection Diagram

LF444AMD/LF444CD/LF444ACN/LF444CN
Dual-In-Line Package



TOP VIEW

Ordering Information

LF444XYZ

X indicates electrical grade

Y indicates temperature range
"M" for military, "C" for commercial

Z indicates package type "D" or "N"

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Circle DATA UPDATE No. 106159

National Semiconductor

July 1982

LH0082 Optical Communication Receiver/Amplifier

General Description

The LH0082 is a general purpose, low-noise, fiber-optic receiver, which may also be used as a fast current to voltage converter, or as a high speed voltage amplifier. The circuit includes a wide-bandwidth FET-input amplifier, a 2.4 volt reference, a comparator with hysteresis, and all the necessary resistors and capacitors for feedback and coupling, all integrated in a hermetic dual-in-line package. The large gain-bandwidth of the preamp enables fast response even with high capacitance photodiodes. A separate analog output permits the reception of analog signals to 20MHz via a fiber-optic link. The internal comparator converts a low level analog signal to a CMOS/TTL compatible logic signal at data rates up to 5Mbits/s NRZ. The LH0082 can be used with an external comparator at data rates to 40Mbits/s.

Features

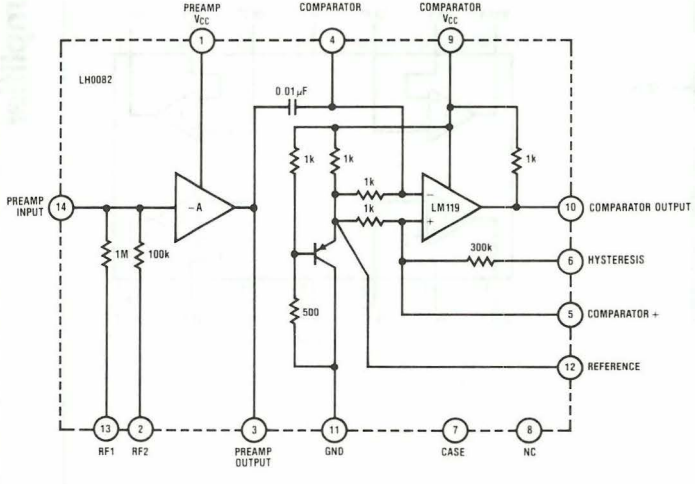
- Single 4.5 to 12 Volt Supply
- 600MHz Unity Gain Bandwidth
- Low Noise
- Low Edge Jitter
- $< 10^{-9}$ Bit Error Rate
- Low Input Bias Current
- Pin Selectable Sensitivity: −45dBm/ −35dBm*
- CMOS/TTL Compatibility
- Can be used with photodiodes, PIN photodiodes, phototransistors, avalanche photodiodes, and photomultipliers
- Hermetic Dual In Line Metal Package
- Highly Versatile Building Block
- > 21dB Dynamic Range

*Assumes 0.5A/W PIN diode input

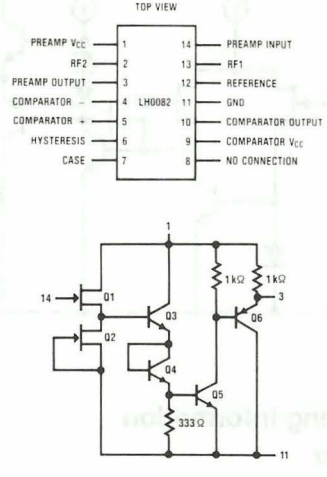
Applications

- Data Terminals
- Secure Communication
- Peripheral Control/Communication
- Video Transmission
- Wideband Amplifier
- High Speed Current to Voltage Converter
- Fiber-Optic Repeater
- Video Amplifier
- Industrial Machine Control

LH0082 Schematic Diagram



Connection Diagram



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DA-B15M72/Printed in U.S.A.

Circle DATA UPDATE No. 106372

National Semiconductor

April 1982

LM1035 Dual DC Operated Tone/Volume/Balance Circuit

General Description

The LM1035 is a DC controlled tone (bass/treble), volume and balance circuit for stereo applications in car radio, TV and audio systems. An additional control input allows loudness compensation to be simply effected.

Four control inputs provide control of the bass, treble, balance and volume functions through application of DC voltages from a remote control system or, alternatively, from four potentiometers which may be biased from a zener regulated supply provided on the circuit.

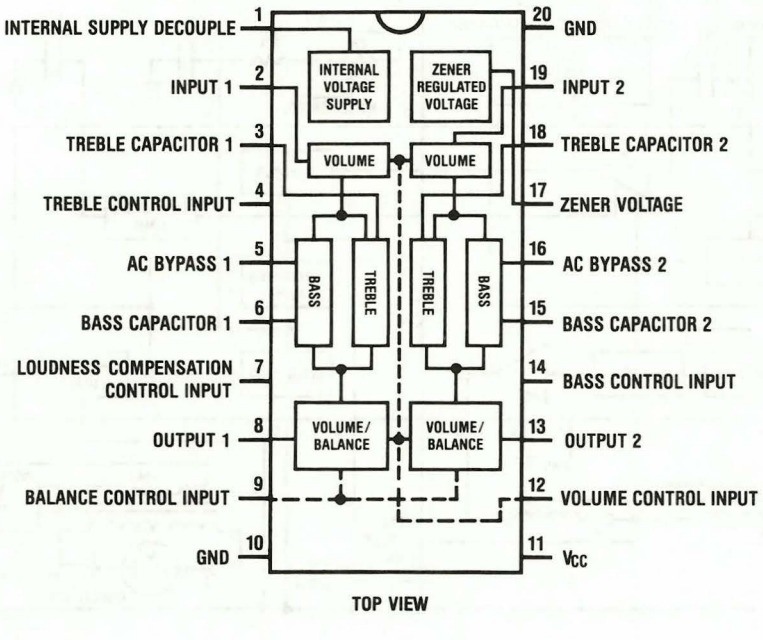
Each tone response is defined by a single capacitor chosen to give the desired characteristic.

Features

- Wide supply voltage range, 8V to 18V
- Large volume control range, 80 dB typical
- Tone control, ± 15 dB typical
- Channel separation, 75 dB typical
- Low distortion, 0.05% typical for an input level of 1 Vrms
- High signal to noise, 80 dB typical for an input level of 1 Vrms
- Few external components required

Block and Connection Diagram

Dual-In-Line Package



TOP VIEW

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Circle DATA UPDATE No. 107295

National Semiconductor

April 1982

LM1812 Ultrasonic Transceiver

General Description

The LM1812 is a general purpose ultrasonic transceiver designed for use in a variety of ranging, sensing, and communications applications. The chip contains a pulse-modulated class C transmitter, a high gain receiver, a pulse modulation detector, and noise rejection circuitry.

A single LC network defines the operating frequency for both the transmitter and receiver. The class C transmitter output drives up to 1A (12W) peak at frequencies up to 325 kHz. The externally programmed receiver gain provides a detection sensitivity of 200 μVp-p. Detection circuitry included on-chip is capable of rejecting impulse noise with external programming. The detector output sinks up to 1A.

Applications include sonar systems, non-contact ranging, and acoustical data links, in both liquid and gas ambients.

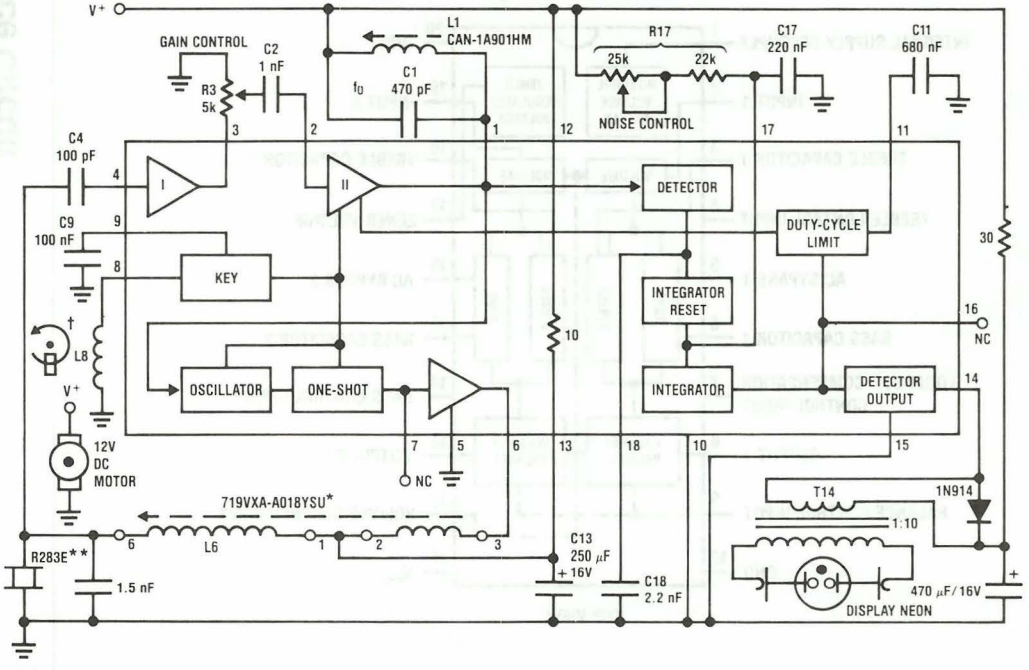
Features

- One or two-transducer operation
- Transducers interchangeable without realignment
- No external transistors
- Impulse noise rejection
- No heat sinking
- Protection circuitry included
- Detector output drives 1A peak load
- Ranges in excess of 100 feet in water, 20 feet in air
- 12W peak transmit power

Applications

- Liquid level measurement
- Sonar
- Surface profiling
- Data links
- Hydroacoustic communications
- Non-contact sensing
- Industrial process control

Typical Application ($V^+ = 12V$)



†Note: Echo returns are displayed by a neon lamp on a motor driven disc. Connections to the neon are made through brushes and slip rings. Rotating with and counterbalancing the neon lamp is a permanent magnet whose field induces a pulse in a stationary coil (L8) as it passes by. This pulse keys the LM1812's transmitter.

*Available from Toko America, Inc., 5520 West Touhy Avenue, Skokie, Illinois 60077 Tel. (312) 677-3640

**Available from Massa Products Corporation, 280 Lincoln Street, Hingham, Massachusetts 02043 Tel. (617) 749-4800

FIGURE 1. 200 kHz Depth Sounder, 5 Feet to 100 Feet

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Circle DATA UPDATE No. 107504

National Semiconductor

June 1982

LM1822 Video IF Amplifier/PLL Detector System

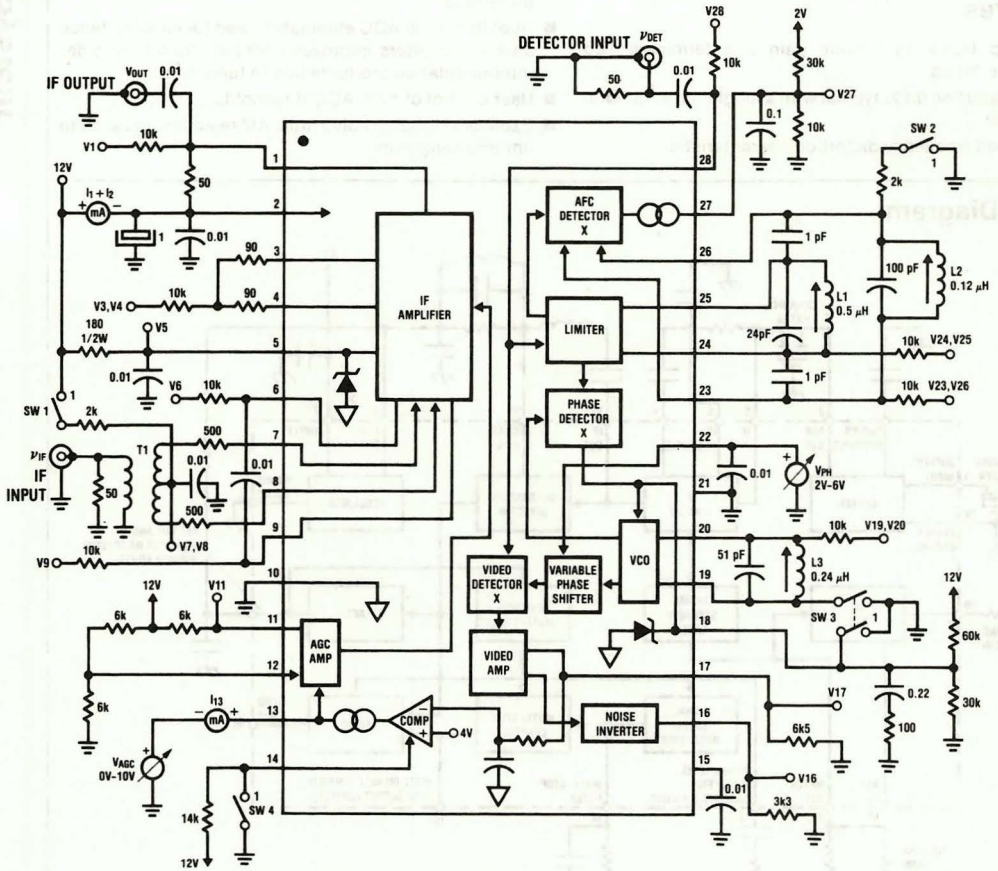
General Description

The LM1822 is a complete video IF signal processing system on a chip. It contains a 5-stage gain-controlled IF amplifier, a PLL synchronous detector with noise inversion, a flexible AFC detector, and gated AGC. This device is suitable for all home receiver and cable IF applications requiring high quality video recovery, including systems operating at 38.9 MHz, 45.75 MHz, 58.75 MHz, and 61.25 MHz.

Features

- Common-base IF inputs for SAW filters
- True synchronous video detector using PLL
- Excellent stability at high system gains
- Noise-averaged gated AGC system
- Superior small-signal detector linearity
- AFC detector with adjustable output bias
- System operation to 70 MHz
- All NPN video amplifiers
- White spot noise inversion
- Adjustable output zero carrier level
- Reverse tuner AGC output

Test Circuit Measure parameters at indicated test points



T1 – 50Ω unbal to bal
Mini-Circuits Lab TM01-1T

L1 – 9 1/2T
L2 – 4 1/2T
L3 – 6 1/2T
} #22 wire on 3/16" form with HF core, shielded

All caps in µF unless noted

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IM-B25M62/Printed in U.S.A.

Circle DATA UPDATE No. 107522

National Semiconductor

PRELIMINARY
August 1982

LM1865/LM1965 Advanced FM IF System

General Description

Reduced external component cost, improved performance, and additional functions are key features to the LM1865/LM1965 FM IF system. The LM1865 is designed for use in electronically tuned radio applications. This version contains both deviation and signal level stop circuitry in addition to an open-collector stop output. The LM1965 is designed for use in manually tuned radios and provides a deviation and signal level mute function in addition to a pin that disables the mute function when grounded.

Features

- On-chip buffer to provide gain and terminate two ceramic filters
- Low distortion 0.1% typical with a single tuned quadrature coil
- Broad off frequency distortion characteristic
- Low THD at minimum AFT offset
- Meter output proportional to signal level
- Mute function with mute disable and soft deviation mute for LM1965
- Stop detector with open-collector output for LM1865
- Adjustable signal level mute/stop threshold, controlled either by ultrasonic noise in the recovered audio or by the meter output
- Adjustable deviation mute/stop threshold
- Separate time constants for signal level and deviation mute/stop
- Dual threshold AGC eliminates need for local/distance switch and offers improved immunity from third order intermodulation products due to tuner overload
- User control of both AGC thresholds
- Excellent signal to noise ratio, AM rejection and system limiting sensitivity

Block Diagram

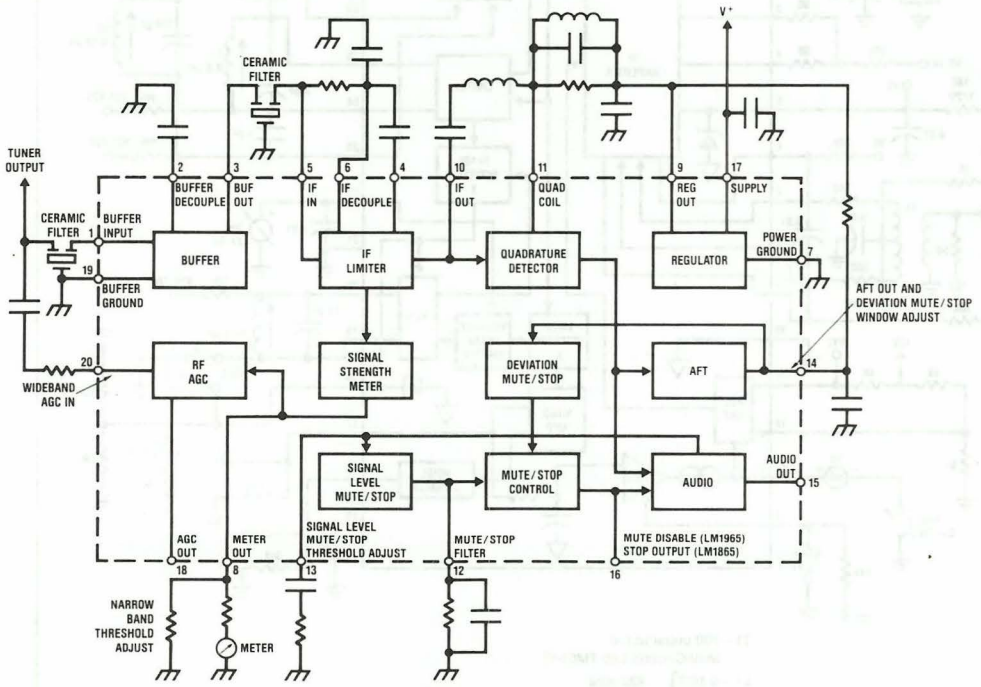

FIGURE 1

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Circle DATA UPDATE No. 107620

National Semiconductor

PRELIMINARY
May 1982

LM1866 Low Voltage AM/FM Receiver

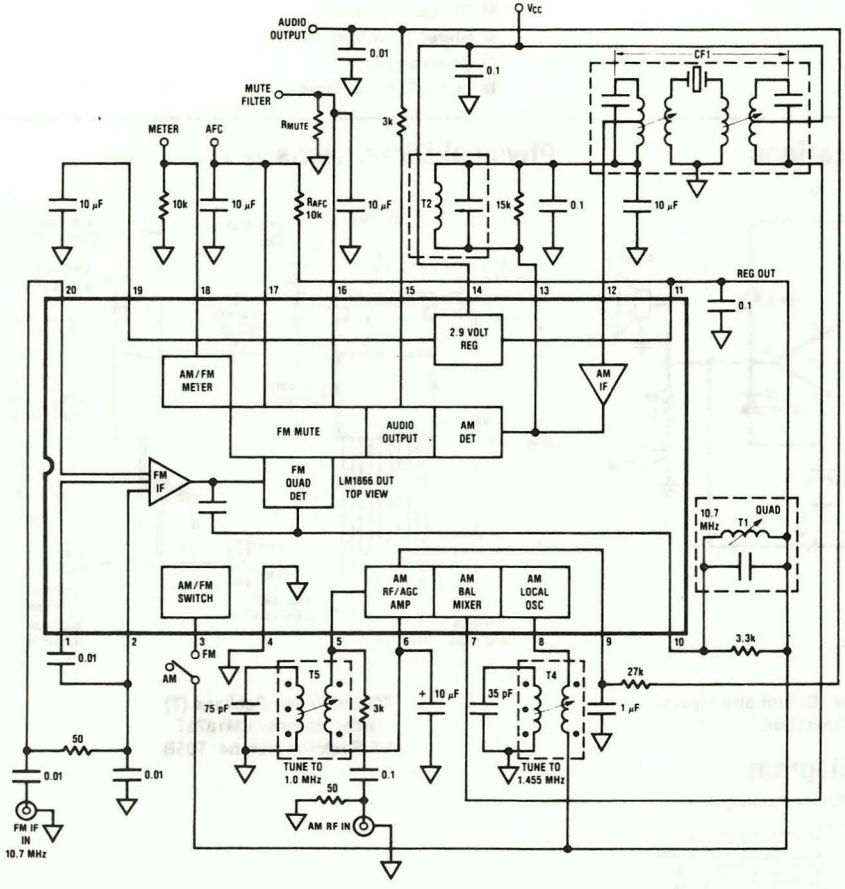
General Description

The LM1866 has been designed for high quality battery powered medium wave AM and FM receiver applications requiring operation down to 3V. The AM section contains a fully balanced, wide dynamic range, gain controlled mixer stage buffered from a single pin local oscillator. A two pin compound IF amplifier and internal detector provide a low distortion high level audio output. An AM/FM signal strength meter voltage is provided to a single output pin. The FM section contains a six stage limiting IF amplifier, quadrature detector, AFC output, deviation audio muting and noise operated audio muting. While designed for the high ripple, high battery impedance conditions found at the end of life for four "C" or "D" cells, the LM1866 will operate equally well at supply voltages up to 15V.

Features

- Operation from 3V to 15V
- Excellent power supply ripple rejection
- Fully balanced, wide dynamic range, AM mixer stage
- Internal AM detector for minimum tweet interference
- Single pole DC AM/FM mode switching
- Six stage FM IF limiting amplifier for excellent AM rejection
- "Soft" FM deviation and noise operated audio muting
- FM quadrature detector
- Single pin AM/FM meter output
- Single pin matched level AM/FM audio output

Block Diagram and Test Circuit



Coil Data:

T2, Toko 159GC-A3785
CF1, Toko CFU-90D
T1, Toko KAC K2318HM
T4 = T5, Toko RBO6A5105

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IM-SVP2.5M52/Printed in U.S.A.

Circle DATA UPDATE No. 107621

National Semiconductor

PRELIMINARY
August 1982

LM1875 20 Watt Power Audio Amplifier

General Description

The LM1875 is a monolithic power amplifier offering very low distortion and high quality performance for consumer audio applications.

The LM1875 delivers 20 watts into a 4Ω or 8Ω load on ±22V supplies. Using an 8Ω load and ±30V supplies, over 30 watts of power may be delivered. The amplifier is designed to operate with a minimum of external components. Device overload protection consists of both internal current limit and thermal shutdown.

The LM1875 design takes advantage of circuit techniques and processing to achieve extremely low levels of distortion even at high levels of output power. Other outstanding features include high gain, fast slew rate and a wide power bandwidth, large output voltage swing, high current capability, and a very wide supply range. The amplifier is also internally compensated and stable for gains of 10 or greater.

Features

- 30 watts of output power
- A_{VO} typically 90 dB
- Low distortion 0.05%, 1 kHz, 20W
- Wide power bandwidth 70 kHz
- Short circuit protection
- Thermal protection with parole circuit
- High current capability 3A
- Wide supply range 20V–60V
- Internal compensation
- 94 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance audio systems
- Bridge amplifiers
- Stereo phonographs
- Servo amplifiers
- Instrument systems

Typical Applications

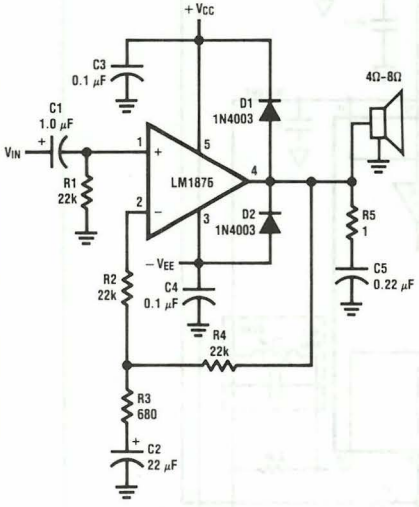
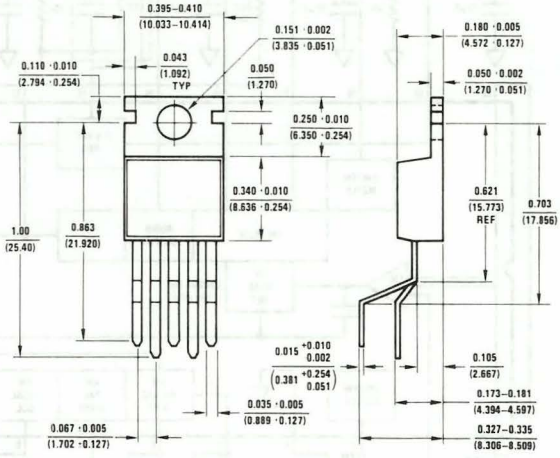


FIGURE 1. Test Circuit and Typical Split Supply Operation

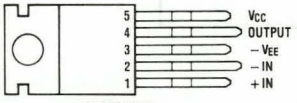
Physical Dimensions inches (millimeters)



TO-220 Power Package (T)
Order Number LM1875T
NS Package Number T05B

Connection Diagram

TO-220 Power Package (T)



FRONT VIEW

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Circle DATA UPDATE No. 107632

National Semiconductor

PRELIMINARY
June 1982

LM1981 AM Stereo Decoder

General Description

The LM1981 is a single IC designed to decode the stereo information which is amplitude and angle modulated on an AM stereo broadcast carrier. It is capable of accepting the 455 kHz (or 262 kHz) IF amplifier output and amplitude detecting the (L + R) mono signal; limiting, detecting and conditioning the (L – R) stereo difference signal; and combining these signals in a suitable matrix to form the left and right channel audio outputs. Other features include an excess phase detector, stereo pilot tone output, stereo/mono blend function, output sample and hold circuits and an internally regulated reference voltage.

The LM1981 is shown in the circuit diagram of *Figure 1*, which includes typical external component values used with the signal format of the Magnavox AM/PM system.

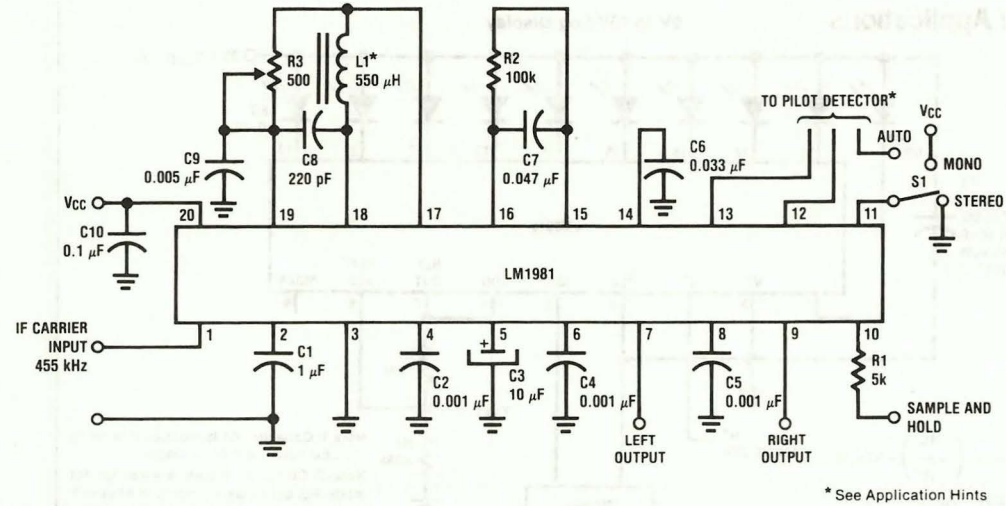
Both left and right channel outputs (pins 7 and 9, respectively) are buffered with sample and hold circuits which can be used to hold the signal level in the presence of a detected noise burst.

The LM1981 AM stereo decoder is available in a 20-pin, molded dual-in-line package.

Features

- Single chip AM stereo decoder
- Minimum external components
- Wide input dynamic range
- Full wave AM detector
- Quadrature PM detection
- Excess phase output
- Noise suppression circuitry
- Stereo pilot tone output
- Stereo/mono auto blend circuit
- Regulated reference output
- Available in plastic 20-pin DIP

Typical Application



* See Application Hints

FIGURE 1. Magnavox System Decoder

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Circle DATA UPDATE No. 107700

National Semiconductor

September 1982

LM3915 Dot/Bar Display Driver

General Description

The LM3915 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing a logarithmic 3 dB/step analog display. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 1 dB.

The LM3915's 3 dB/step display is suited for signals with wide dynamic range, such as audio level, power, light intensity or vibration. Audio applications include average or peak level indicators, power meters and RF signal strength meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The LM3915 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

The LM3915 is very versatile. The outputs can drive LCDs, vacuum fluorescents and incandescent bulbs as well as LEDs of any color. Multiple devices can be cascaded for a dot or bar mode display with a range of 60 or 90 dB. LM3915s can also be cascaded with LM3914s for a linear/log display or with LM3916s for an extended-range VU meter.

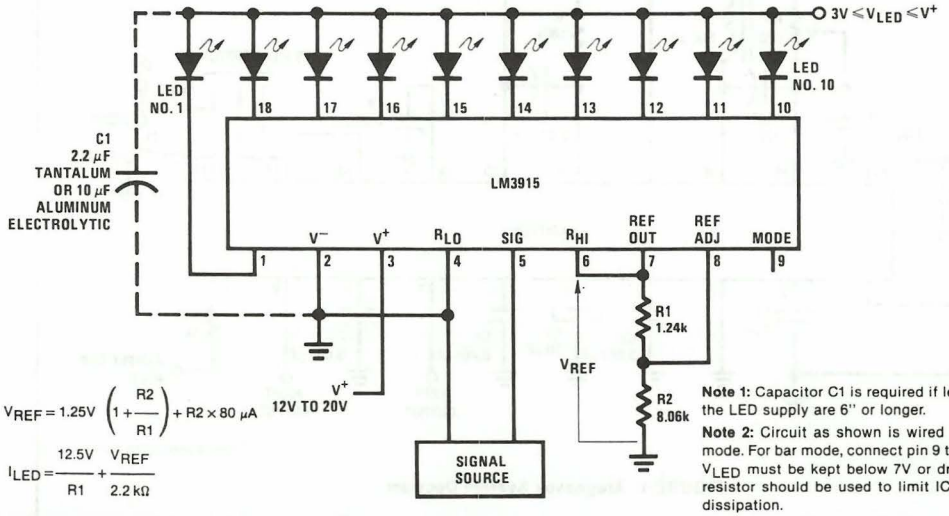
Features

- 3 dB/step, 30 dB range
- Drives LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 90 dB
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of 3V to 25V
- Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3915 is rated for operation from 0°C to +70°C. The LM3915N is available in an 18-lead molded DIP package and the LM3915J comes in the 18-lead ceramic DIP.

Typical Applications

0V to 10V Log Display



Note 1: Capacitor C1 is required if leads to the LED supply are 6" or longer.

Note 2: Circuit as shown is wired for dot mode. For bar mode, connect pin 9 to pin 3. V_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

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IM-B25M92/Printed in U.S.A.

Circle DATA UPDATE No. 108232

National Semiconductor

March 1982

LT10 Linear Bipolar Power Transistor

general description

The LT10 is an entirely new power transistor design that combines exceptional ruggedness with an $f_T > 40$ MHz. Forward biased secondary breakdown has been virtually eliminated so that over 200W can be dissipated for durations in excess of one second at voltages up to 200V. Saturation voltage at 12A is under 1.5V.

This unique combination of characteristics is achieved using ion implanted base ballasting.† The ballast is voltage modulated by depletion with collector-base bias to increase ballast resistance as voltage is increased. This insures adequate ballasting at high voltage where it is needed, while limiting ballast losses at low voltage.

Reliability is enhanced because hot-spotting is avoided. Therefore, thermal resistance remains low even at maximum voltage. A molybdenum interface between the silicon die and the copper heat spreader matches expansion coefficients, eliminating thermal fatigue failures. Further, oxide-passivated junctions insure stability of the low leakage currents.

These transistors are expected to find applications in power amplifiers, regulators, disc head positioners, deflection-yoke drivers for CRT displays, or other places where the ability to withstand the simultaneous application of high voltage and high current is important. The frequency response is an added bonus, especially in stabilizing feedback circuits, improving transient response, or avoiding quiescent current runaway in class-B amplifiers at high frequencies. Significantly, the base ballast resistance effectively suppresses the parasitic oscillations usually encountered with fast transistors.

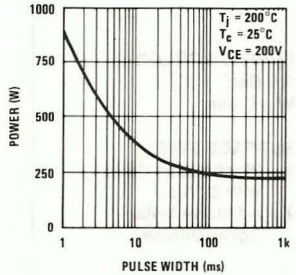
†R.J. Widlar, "Controlling Secondary Breakdown in Bipolar Power Transistors," National Semiconductor TP-16.

maximum ratings

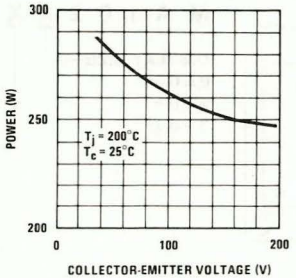
parameter		conditions	LT10-140V	LT10-200V
full power collecter voltage	$V_{CE(max)}$	$P_D \leq P_{D(max)}$, $T_j \leq 200°C$	140V	200V
emitter-base voltage	V_{EBO}	$I_C = 0$	5V	
collector current	I_C	continuous $t_{ON} \leq 5$ ms, $t_{OFF} \geq 50$ ms	12A 25A	
base current	I_B	continuous	5A	
dc power dissipation	$P_{D(max)}$	$V_{CE} \leq V_{MAX}$, $T_C \leq 25°C$	200W	
operating temperature range	T_j		−65°C to 200°C	
storage temperature range	T_{STG}		−65°C to 200°C	

typical characteristics

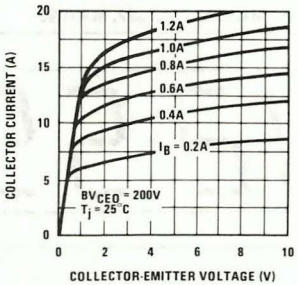
pulse power



dc power



collector



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Circle DATA UPDATE No. 108470

National Semiconductor

June 1982

MA1020, MA1022, MA1023 Series Low Cost Digital LED Clock Module

General Description

The MA1020, MA1022, MA1023 series electronic digital clock modules feature four-digit LED displays; only a transformer and setting switches are required to produce a low cost, full featured movement for use in alarm clock, clock radio, instrument panel clock and appliance timer applications. Advanced packaging techniques allow minimum overall size and high reliability.

Key features include multiple 9-minute snooze, "one-finger" sleep setting, easy to use fast and slow setting controls, seconds display, PM, power-fail and alarm-on indicators and time-set lockout. The unit includes components for on-board radio switching, speaker drive (an 800 Hz nominal alarm-tone output is gated at a 2 Hz rate) and battery-powered back-up oscillator for timekeeping during power loss. Maximum flexibility is provided by user-programmable 12/24-hour display, 50/60 Hz input and fixed or flashing colon options. In addition, the display brightness level can be varied with a potentiometer for continuous control, or an SPST switch for bright/dim control.

Applications

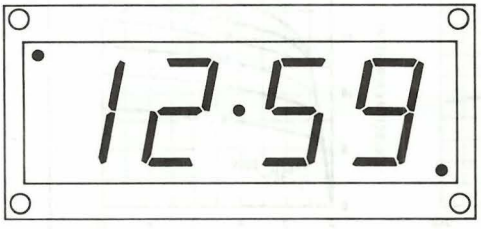
- Clock radio timers
- Alarm clocks
- Desk clocks
- TV, stereo timers
- Instrument panel clocks

Features

- Available in three display sizes: 0.84", 0.7" or 0.5" with or without red or clear lens
- "One finger" 59-minute sleep counter setting
- Multiple 9-minute snooze counter
- 24-hour alarm with on-off control
- PM, colon, and alarm on indicators
- Entire display flashes to indicate power loss
- Simple fast/slow setting controls
- Time-set lockout feature eliminates accidental time-setting without inhibiting alarm or sleep setting
- 5 display modes (time, seconds, alarm, sleep and lamp test)
- User-selectable 12/24-hour, 50/60 Hz and fixed/flashing colon options
- Leading zero blanking
- Requires only the addition of transformer and setting switches for complete system
- Low power consumption
- Direct-drive LED display—no RFI
- Continuous "two-level" or automatic display brightness control capability
- Back-up oscillator allows continuous timekeeping during power-line failure with an external 9 volt battery and 5 MΩ potentiometer
- 800 Hz (nominal) alarm tone output, gated at a 2 Hz rate
- Includes components for alarm clock (8Ω speaker drive) or clock radio (power switch) applications
- 24-hour output signal for optional calendar circuit
- Separate inputs for all settings and display modes

Display Outline

MA1020, MA1022, MA1023



Ordering Information

M A 1 0 2 X X X

DISPLAY SIZE
0 = 0.84"
2 = 0.5"
3 = 0.7"

SURFACE TYPE
L = Plastic Lens Cover with Diffuser
Z = Adhesive Mylar Cover/Diffuser

SURFACE COLOR
R = Red
W = Clear

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IM-B25M62/Printed in U.S.A.

Circle DATA UPDATE No. 108636

MA1020, MA1022, MA1023 Series Low Cost Digital LED Clock Module

National Semiconductor

June 1982

MA1033 12 V_{DC} Automotive/Instrument Clock Module

General Description

The MA1033 is an electronic digital automotive clock module featuring 4-digit LED displays. It is designed to offer the user a low cost automotive or instrument clock module with electronic assembly capability. A minimum number of discrete components are needed to form a complete digital clock for 12 V_{DC} instrument panel applications. Additional components are needed to fully protect against automotive transients and battery reversal conditions.

Key features include easy-to-use fast and slow setting controls, 0.3 inch display size, low power consumption, leading zero blanking, power loss indication, and direct drive LED display/no RFI. The display brightness can be varied with a single external potentiometer.

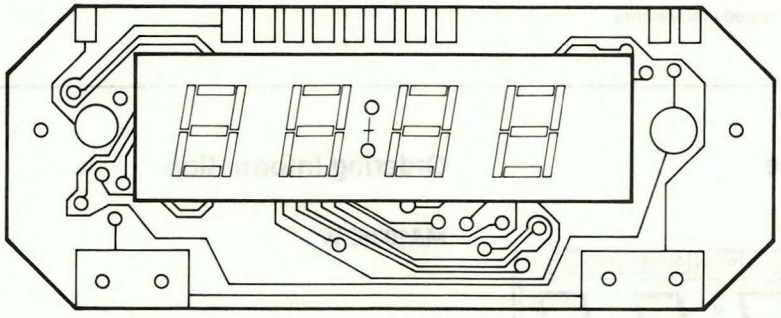
Functional Features

- Available in 0.3" display size with adhesive mylar cover/diffuser and clear surface color
- Entire display flashes to indicate power loss
- Simple fast/slow setting controls
- Leading zero blanking
- Low power consumption
- Direct drive LED display/no RFI
- Display brightness control

Applications

- In-dash auto clocks
- After-market auto/recreational vehicle clocks
- Aircraft-marine clocks
- 12 V_{DC} operated instruments
- Portable/battery powered instruments

Display Outline



MA1033 12 V_{DC} Automotive/Instrument Clock Module

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Circle DATA UPDATE No. 108661

National Semiconductor

June 1982

MA1036 12 V_{DC} Automotive/Instrument Clock Module

General Description

The MA1036 is an electronic digital clock/timer module featuring 4-digit LED displays. This is designed to offer a low cost digital clock/timer module for the user with electronic assembly capability. In addition to a transformer and setting switches, a minimum number of discrete components are required to produce a full-featured movement for use in alarm clock, clock radio, instrument panel clock and appliance timer applications. Advanced packaging techniques allow minimum overall size and high reliability in finished products.

Key features include multiple 9-minute snooze; "one finger" sleep setting; easy to use fast and slow setting controls; five display modes (time, seconds, alarm, sleep and lamp test); PM alarm ON and LED colon indicators; power failure indication and time-set lockout. All models are designed to generate a selectable frequency alarm tone output gated at a 2 Hz rate (provided the user adds an external resistor and capacitor). Maximum flexibility is provided by optional 12 or 24-hour display format, and fixed or blinking colon indicator. The display brightness level can be varied with a single external potentiometer for continuous control.

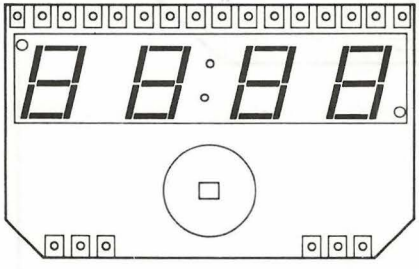
Applications

- In-dash auto clocks
- After-market auto/recreational vehicle clocks
- Aircraft-marine clocks
- 12 V_{DC} operated instruments
- Portable/battery powered instruments

Functional Features

- Available in 0.3″ display size with adhesive mylar cover/diffuser and clear surface color
- Low power consumption
- Direct drive LED display/no RFI
- Display brightness control
- Selectable frequency alarm tone output, gated at a 2 Hz rate, provides an easy interface to an 8Ω speaker for alarm clock application
- DC level sleep output provides an easy interface for clock radio and timer applications
- 24-hour output for an optional calendar circuit
- Separate inputs for all settings and display modes
- "One finger" 59-minute sleep counter setting
- Multiple 9-minute snooze control
- 24-hour alarm with ON/OFF control
- PM, colon and alarm ON LED indicators
- Entire display flashes to indicate power loss
- Simple fast/slow setting controls
- Time-set "lockout" feature eliminates accidental time-setting without inhibiting alarm or sleep settings
- Five display modes (time, seconds, alarm, sleep and lamp test)
- Leading zero blanking

Display Outline



Ordering Information

MA1036ZW

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Circle DATA UPDATE No. 108664

MA1036 12 V_{DC} Automotive/Instrument Clock Module

National Semiconductor

June 1982

MA1122 Series High Efficiency Low Cost Digital LED Clock Module

General Description

The MA1122 electronic digital clock module features a four-digit LED display in high efficiency red, green or yellow options; only a transformer and setting switches are required to produce a low cost, full featured movement for use in alarm clock, clock radio, instrument panel clock and appliance timer applications. Advanced packaging techniques allow minimum overall size and high reliability.

Key features include multiple 9-minute snooze, "one-finger" sleep setting, easy to use fast and slow setting controls, seconds display, PM, power-fail and alarm-on indicators and time-set lockout. The unit includes components for on-board radio switching, speaker drive (an 800 Hz nominal alarm-tone output is gated at a 2 Hz rate) and battery-powered back-up oscillator for timekeeping during power loss. Maximum flexibility is provided by user-programmable 12/24-hour display, 50/60 Hz input and fixed or flashing colon options. In addition, the display brightness level can be varied with a potentiometer for continuous control, or an SPST switch for bright/dim control.

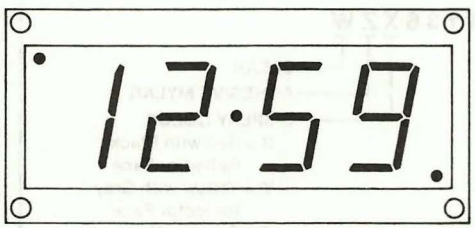
Applications

- Clock radio timers
- Alarm clocks
- Desk clocks
- TV, stereo timers
- Instrument panel clocks

Features

- 0.5 inch red, green or yellow LED display with or without lens
- "One finger" 59-minute sleep counter setting
- Multiple 9-minute snooze counter
- 24-hour alarm with on-off control
- PM, colon, and alarm indicators
- Entire display flashes to indicate power loss
- Simple fast/slow setting controls
- Time-set lockout feature eliminates accidental time-setting without inhibiting alarm or sleep setting
- 5 display modes (time, seconds, alarm, sleep and lamp test)
- User-selectable 12/24-hour, 50/60 Hz and fixed/flashing colon operation
- Leading zero-blanking
- Requires only the addition of transformer and setting switches for complete system
- Low power consumption
- Direct-drive LED display—no RFI
- Continuous "two-level" or automatic display brightness control capability
- Back-up oscillator allows continuous timekeeping during power-line failure with an external 9 volt battery and 5 MΩ potentiometer
- 800 Hz (nominal) alarm tone output, gated at a 2 Hz rate
- Includes components for alarm clock (8Ω speaker drive) or clock radio (power switch) applications
- 24-hour output signal for optional calendar circuit
- Separate inputs for all settings and display modes

Display Outline



Ordering Information

M A 1 1 2 2 X X X

DISPLAY SIZE: 0.5"

SURFACE COLOR
R = Red
W = Clear

SURFACE TYPE
L = Plastic Lens Cover with Diffuser
Z = Adhesive Mylar Cover/Diffuser

DISPLAY COLOR
R = Red with Black Reflector Face
Y = Yellow with Gray Reflector Face
G = Green with Gray Reflector Face

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Circle DATA UPDATE No. 108672

National Semiconductor

June 1982

MA1136 12 V_{DC} Automotive/Instrument Clock Module

General Description

The MA1136 is an electronic digital automotive clock module featuring 4-digit high efficiency LED displays. It is designed to offer the user a low cost automotive or instrument clock module with electronic assembly capability. A minimum number of discrete components are needed to form a complete digital clock for 12 V_{DC} instrument panel applications. Additional components are needed to fully protect against automotive transients and battery reversal conditions.

The MA1136 may also be used with switches to produce a full-featured movement for use in DC operated alarm clock, clock radio, and appliance timer applications. Advanced packaging techniques allow minimum overall size and high reliability in finished products.

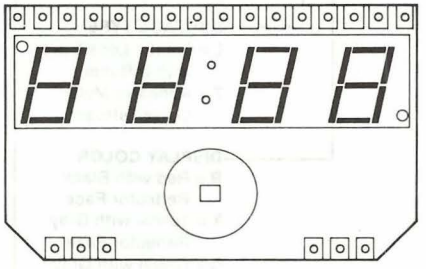
Applications

- In-dash auto clocks
- After-market auto/recreational vehicle clocks
- Aircraft-marine clocks
- 12 V_{DC} operated instruments
- Portable/battery powered instruments

Functional Features

- High intensity
- Available in 0.3" display size with adhesive mylar cover/diffuser and clear surface color
- Low power consumption
- Direct drive LED display/no RFI
- Display brightness control
- Selectable frequency alarm tone output, gated at a 2 Hz rate, provides an easy interface to an 8Ω speaker for alarm clock application
- DC level sleep output provides an easy interface for clock radio and timer applications
- 24-hour output for an optional calendar circuit
- Separate inputs for all settings and display modes
- "One finger" 59-minute sleep counter setting
- Multiple 9-minute snooze control
- 24-hour alarm with ON/OFF control
- PM, colon and alarm ON LED indicators
- Entire display flashes to indicate power loss
- Simple fast/slow setting controls
- Time-set "lockout" feature eliminates accidental time-setting without inhibiting alarm or sleep settings
- Five display modes (time, seconds, alarm, sleep and lamp test)
- Leading zero blanking

Display Outline



Ordering Information

M A 1 1 3 6 X Z W

- **W** — **CLEAR**
- **Z** — **ADHESIVE MYLAR**
- **X** — **DISPLAY COLOR**
  - **R** = Red with Black Reflector Face
  - **Y** = Yellow with Gray Reflector Face
  - **G** = Green with Green Reflector Face

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IM-B25M62/Printed in U.S.A.

Circle DATA UPDATE No. 108674

National Semiconductor

June 1982

MA1142/MA1143 Series Low Cost Digital High Efficiency LED Clock Modules

General Description

The MA1142/MA1143 series of 4-digit LED electronic digital clock modules is designed to offer low cost in a digital clock assembly with a choice of three colors. In addition to a transformer and setting switches, a minimum number of discrete components are required to produce a full-featured movement for use in alarm clock, clock radio, instrument panel clock and appliance timer applications. Advanced packaging techniques guarantee minimum overall size and high reliability in finished products.

Key features include red, green or yellow display; multiple 9-minute snooze; "one finger" sleep setting; easy to use "fast and slow" setting controls; five display modes (time, seconds, alarm, sleep and lamp test); PM, alarm ON and LED colon indicators; power failure indication; time-set lockout; and back-up oscillator for battery powered timekeeping during power loss. All models are designed to generate a selectable frequency alarm tone output gated at a 2 Hz rate (provided the user adds an external resistor and capacitor). Worldwide market flexibility is provided by user-programmable 12 or 24-hour display format, 50 Hz or 60 Hz input frequency selection and fixed or blinking colon indicator. The display brightness level can be varied with a single external potentiometer for continuous control.

Features

- Red, green or yellow LED display
- Available in two display sizes, 0.7" or 0.5", with or without clear or red lens filter
- "One finger" 59-minute sleep counter setting
- Multiple 9-minute snooze control
- 24-hour alarm with ON/OFF control
- PM, colon and alarm ON LED indicators
- Entire display flashes to indicate power loss
- Simple fast/slow setting controls
- Time set lockout feature eliminates accidental time-setting without inhibiting alarm or sleep settings
- Five display modes (time, seconds, alarm, sleep and lamp test)
- User selectable 12/24-hour, 50 Hz/60 Hz and fixed or flashing colon operation
- Leading zero blanking
- On board zener protection of LEDs
- Direct drive LED display/produces no RFI
- Display brightness control
- Back-up oscillator allows continuous timekeeping during power-line failure with an external 9V battery and 5 MΩ potentiometer

Applications

- Clock radio timers
- Alarm clocks
- Desk clocks
- TV, stereo timers
- Appliance timers
- Instrument panel clocks

Display Outline

MA1142/MA1143

Ordering Information

M A 1 1 4 X X X X

DISPLAY SIZE
2 = 0.5"
3 = 0.7"

LENS SURFACE COLOR
R = Red
W = Clear

SURFACE TYPE
Z = Adhesive Mylar
L = Plastic Lens Cover with Diffuser

DISPLAY COLOR
Y = Yellow
G = Green
R = Red

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Circle DATA UPDATE No. 108677

National Semiconductor

PRELIMINARY
June 1982

MA2016 16,384 × 8-Bit CMOS Static RAM Module

General Description

The MA2016 consists of eight 2k × 8-bit CMOS RAMs along with an address decoder capable of decoding up to a 128k × 8-bit low power CMOS RAM. It operates on a single 5V power supply and is able to retain data down to 2V. The MA2016 does not require a refresh and all inputs and outputs are TTL compatible. Multiple MA2016 modules may be stacked in a piggyback fashion or laid out in any manner desired. The low power requirements and versatile layout make the MA2016 very useful for low power hand-held battery powered applications.

Applications

- Portable terminals
- Hand-held devices
- Pos terminals
- Remote instrumentation
- Process controllers
- Microcomputer memory

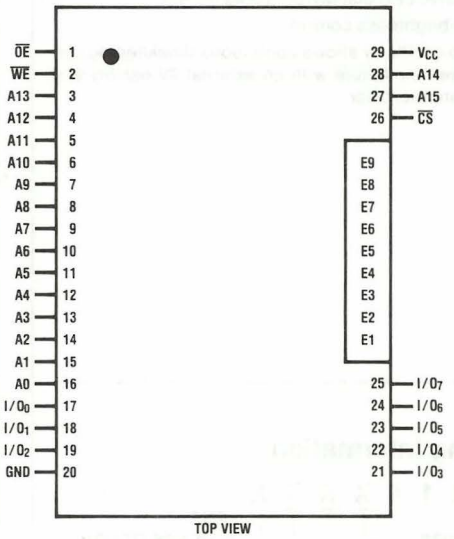
Features

- 16k × 8-bits fully decoded
- Outputs directly TTL compatible
- Low power—typical 400 mW
- 250 ns access time
- Static operation—no clocks or refreshing required
- Single 5V supply ± 10%
- 2V minimum for data retention
- TRI-STATE® outputs for bus operation
- Common data I/O pins
- Separate OE pin
- Internal power supply decoupling

Ordering Information

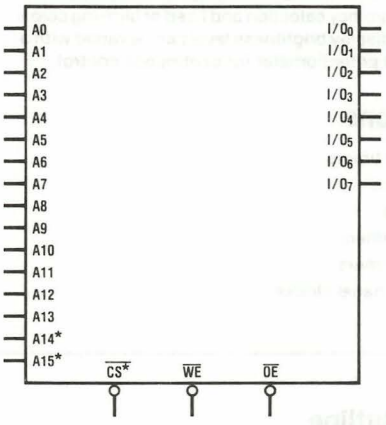
MA2016

Connection Diagram



TOP VIEW

Logic Symbol



* active state user selectable

Pin Names

$\overline{CS}$	Chip Select Input (user programmable)
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O_0-I/O_7	Data Inputs/Outputs
A0-A15	Address Inputs (A14, A15 Block Select, user programmable)
V_{CC}	Power (typical 5V)
GND	Ground

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Truth Table

$\overline{CS}$*	$\overline{WE}$	$\overline{OE}$	I/O	Mode
H	X	X	Hi-Z	Standby
L	H	L	D_{OUT}	Read
L	H	H	Hi-Z	Read
L	L	X	D_{IN}	Write

* $\overline{CS}$ state is user selectable. Table shown with jumper E7 to E8 and E4 to E5 installed.

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Circle DATA UPDATE No. 108678

National Semiconductor

PRELIMINARY
May 1982

MA3051 12 V_{DC} Automotive/Instrument Clock and Elapsed Timer Module

General Description

The MA3051 12 V_{DC} automotive/instrument clock module combines the MM53124 monolithic MOS/LSI clock and elapsed timer circuit, a 4-digit 0.236″ green vacuum fluorescent display, a 4.194 MHz crystal and supporting components to form a complete digital clock and elapsed timer for 12 V_{DC} application. The module is fully protected against automotive transients and battery reversal conditions with timekeeping maintained down to 8.5 V_{DC}. Interconnections are simplified through use of a 5-pin connector. The bright green display color is filterable to various shades in the blue, green, blue-green and yellow color range. The display brightness is automatically reduced to approximately 25% when park lights or headlights are on. When ignition (IGN) and park lights are both off, all input switches are disabled and the display is turned off to conserve power. In this mode the display may be activated by closing the display switch. The display features leading zero blanking and, in the elapsed time mode, has a blinking colon activity indicator when elapsed time exceeds 60 minutes.

Features

- Ideal for automotive applications
- Operates from 12 V_{DC} supply
- Bright 0.236″ green vacuum fluorescent display
- Internal crystal timebase
- ± 0.5 second/day accuracy (typical, at room temperature)
- Protected against automotive voltage transients and reversals
- Timekeeping maintained to 8.5 V_{DC}; memory to 6.5 V_{DC}
- Automatic display brightness control logic
- Display color filterable to blue, blue-green, green and yellow
- Complete clock and elapsed timer
- Convenient time setting controls at a 2 Hz rate with no roll-over
- Compact size, built-in connector
- Low standby power consumption
- Lockout of time setting when both ignition and park lights are off

Applications

- In-dash auto clocks
- After-market auto/recreational vehicle clocks
- Aircraft-marine clocks
- 12 V_{DC} operated instruments
- Portable/battery powered instruments

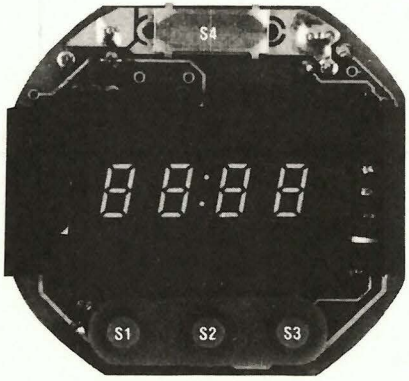
Operating Guide

A. To set time (if ignition is on *or* park lights are on)
   1. Set hours: push S3, then S2 to increment hours
   2. Set minutes: push S3, then S2 to increment minutes (If hours are correct, push S3 two times, then S2 to increment minutes)
   3. Push S3 to return to display time mode

B. To use elapsed timer (if ignition is on *or* park lights are on)
   1. Push S1 (enables timer)
   2. Push S3 (starts timer)
   3. Pushing S2 stops timer and holds value
   4. Pushing S1 and S3 together resets timer
   5. Pushing S1 returns to display time mode

C. If the ignition and the park lights are both off the above functions can be performed by depressing and holding S4. The time will be displayed while S4 is depressed. All functions are disabled when S4 is released.

D. Pushing S4 alone will have no effect if the ignition or the park lights are on



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IM-B25M52/Printed in U.S.A.

Circle DATA UPDATE No. 108680

National Semiconductor

June 1982

MA6013 3-Digit Electronic Up/Down Counter Module

General Description

The MA6013 is an electronic up/down counter module featuring a 3-digit LED display. The display consists of monolithic red digits magnified by a clear bubble lens which produces an apparent digit height of 0.180″ (4.44 mm). Designed for applications in tape recording systems, a four-bit prescaler (divide by 16) is incorporated in the system design. Input pulses, which may be derived from electromechanical, optical or electronic sources, are fed into two input lines designated as A CLOCK and B CLOCK. A pulse shaper network consisting of two Schmitt triggers and an R-S flip-flop, detects a pulse of 10 μs or greater and generates a bounce free clock signal for each valid input. To effect either an up count or a down count, the sequence of input pulses must be B followed by A, and the counter will increment or decrement one unit for each 16 clock cycles. The increment or decrement mode is determined by the state of the up/down input. PMOS ion implantation technology is used on the integrated circuit.

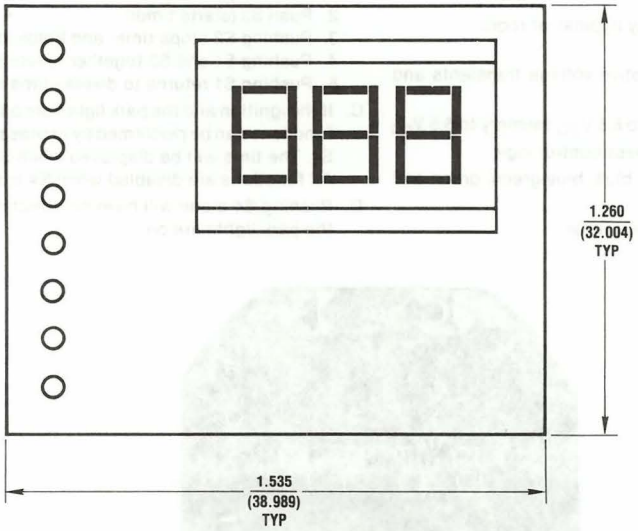
Features

- Small size
- 0.180″ (4.44 mm) apparent digit height
- ±17° viewing angle
- No leading zero blanking
- Simple to use
- Power-on reset

Applications

- Tape recording systems
- Up/down counter
- Toys and games

Display Outline



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Circle DATA UPDATE No. 108725

MA6013 3-Digit Electronic Up/Down Counter Module

National Semiconductor

July 1982

MM5458, MM5459 Digital Alarm Clocks

General Description

The MM5458, MM5459 digital alarm clock radio chips are monolithic MOS integrated circuits utilizing N-channel low-threshold enhancement mode and ion-implanted depletion mode devices.

Each circuit contains all the logic necessary for a digital clock with sleep and alarm control and is intended for clock-radio applications.

Real-time and alarm time are displayed in hours/minutes and sleep time is displayed in minutes when setting the sleep counter.

An alarm output is provided that "beeps" a 960 Hz tone gated by 2 Hz rate when the Alarm Set time and the real-time matches. A sleep output that provides a DC level is used to control the radio. It is activated with the alarm output or programmed via the sleep counter to turn OFF from 0 to 59 minutes after the sleep counter is set.

A snooze feature is provided for a 9-minute recurrence of the alarm after it has sounded. Setting is done via the standard fast and slow Set buttons when in the Time Set, Alarm Set, or Sleep Set modes. These control inputs are TRI-STATE® inputs to reduce pin count.

The 50/60 Hz clock selects what segment data is on the outputs, i.e., a duplex LED display interface. A standby battery input compares the battery voltage to the transformer voltage and switches the time base reference from the 50/60 Hz input to the alarm oscillator in the event of an AC power failure.

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The MM5458 is bonded in a 24-pin package and is capable of 24-hour/50 Hz, 12-hour/60 Hz and 12-hour/50 Hz operations.

The MM5459 is bonded in a 22-pin package and is a 12 hour/60 Hz version of the MM5458.

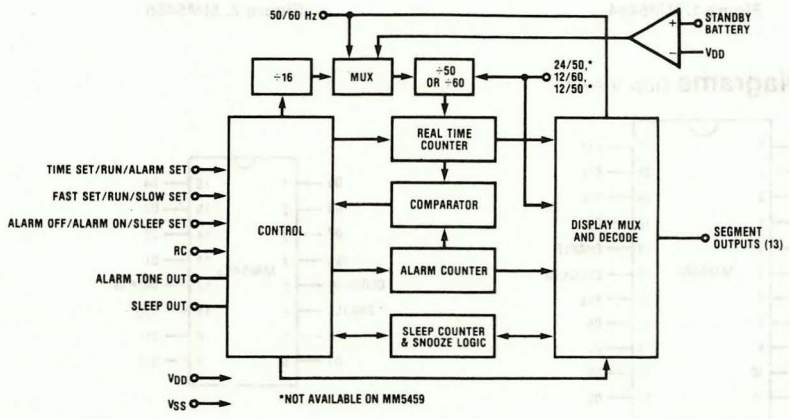
Features

- Duplex LED display drive
- Fast/slow set capability
- 24-hour alarm
- "Snooze" function (9 minutes)
- On-chip alarm oscillator
- Alarm tone output gated at a 2 Hz rate
- Standby battery operation
- Power fail indication — entire display flashes at a 1 Hz rate
- Automatic power-on reset
- PM display indicator
- Presettable 59-minute sleep timer

Applications

- Alarm Clocks
- Desk clocks
- Clock radios
- Automobile clocks
- Stopwatches
- Industrial clocks
- Portable clocks
- Timers

Block Diagram



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Circle DATA UPDATE No. 110000

National Semiconductor

April 1982

MM5484, MM5485 16-, 11-Segment LED Display Drivers

General Description

The MM5484, MM5485 are low threshold N-channel metal gate circuits using low threshold enhancement and ion implanted depletion devices. the MM5484 is available in a 22-pin molded package and is capable of driving 16 LED segments while the MM5485 is available in a 16-pin molded package and is capable of driving 11 LED segment outputs.

Features

- Serial data input
- Wide power supply operation
- 16 or 11 outputs, 15mA sink capability
- MM5484 is cascadeable
- TTL compatibility
- No load signal required
- Non multiplex display
- 2½ digit capability—MM5484
  1½ digit capability—MM5485

Applications

- COPS™ or microprocessor displays
- Instrumentation readouts
- Industrial control indicator
- Relay driver

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Block Diagrams

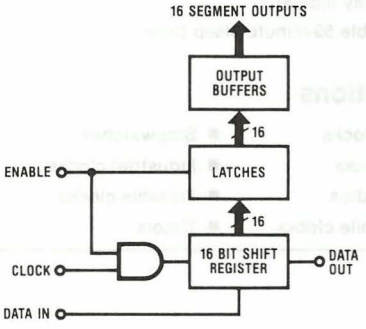


Figure 1. MM5484

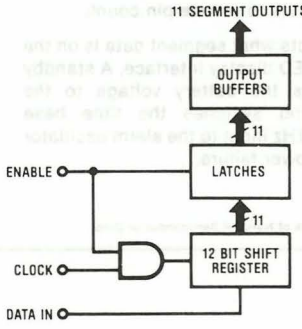
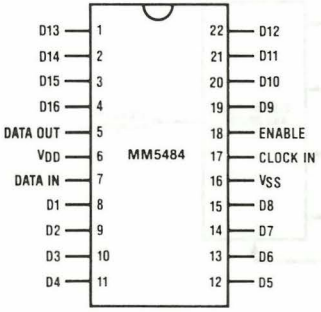


Figure 2. MM5485

Connection Diagrams (Top Views)



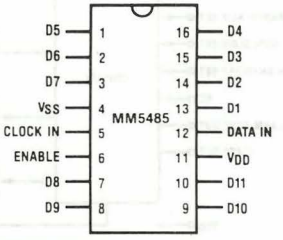


Figure 4.

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Circle DATA UPDATE No. 110008

National Semiconductor

PRELIMINARY
May 1982

MM54HC00/MM74HC00 Quad 2-Input NAND Gate
MM54HC10/MM74HC10 Triple 3-Input NAND Gate
MM54HC20/MM74HC20 Dual 4-Input NAND Gate
MM54HC30/MM74HC30 8-Input NAND Gate
MM54HC133/MM74HC133 13-Input NAND Gate

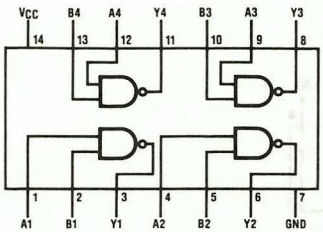
MM54HC00/MM74HC00, MM54HC10/MM74HC10, MM54HC20/MM74HC20, MM54HC30/MM74HC30, MM54HC133/MM74HC133

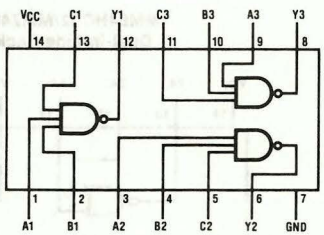
General Description

These logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LSTTL loads (8 LSTTL loads for 54HC). The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

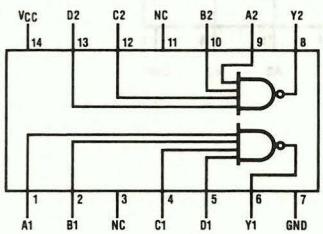
Connection Diagrams

MM54HC00/MM74HC00
$Y = \overline{AB}$



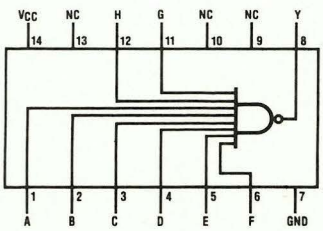


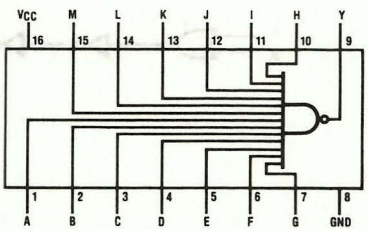
MM54HC10/MM74HC10
$Y = \overline{ABC}$



MM54HC20/MM74HC20
$Y = \overline{ABCD}$

MM54HC30/MM74HC30
$Y = \overline{ABCDEFGH}$





MM54HC133/MM74HC133
$Y = \overline{ABCDEFGHIJKLMN}$

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Circle DATA UPDATE No. 111610

National Semiconductor

August 1982

MM54HC02/MM74HC02 Quad 2-Input NOR Gate

General Description

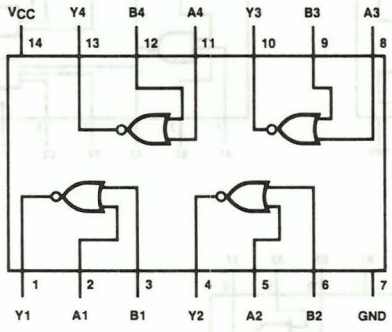
These NOR gates utilize silicon gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads (8 LS-TTL loads for the 54HC). The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8ns
- Wide power supply range: 2-6V
- Low quiescent supply current: 20μA maximum (74 series)
- Low input current: 1μA max
- High output current: 4mA minimum (74 series)

Connection Diagram

MM54HC02/MM74HC02
Dual-In-Line Package



Logic Diagram

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Circle DATA UPDATE No. 111603

National Semiconductor

April 1982

MM58174A Microprocessor-Compatible Real-Time Clock

General Description

The MM58174A is a low-threshold metal-gate CMOS circuit that functions as a real-time clock and calendar in bus-oriented microprocessor systems. The device includes an interrupt timer which may be programmed to one of three times. Time-keeping is maintained down to 2.2V to allow low power standby battery operation. The timebase is generated from a 32768Hz crystal-controlled oscillator.

Features

- Microprocessor compatible
- Tenths of seconds, seconds, tens of seconds, minutes, tens of minutes, day of week, days, tens of days, months, tens of months, independent registers
- Automatic leap year calculation
- Internal pull-ups to safeguard data
- Protection for read during data changing
- Fast access time (500ns)
- Independent interrupt system with open drain output
- TTL compatible
- Low power standby operation (2.2V, 10μA)
- Low cost internally biased oscillator
- Low cost 16-pin dual-in-line package
- Available for commercial and military temperature ranges

Applications

- Point-of-sale terminals
- Word processors
- Teller terminals
- Event recorders
- Microprocessor-controlled instrumentation
- Microprocessor time clock
- TV/VCR reprogramming
- Intelligent telephone

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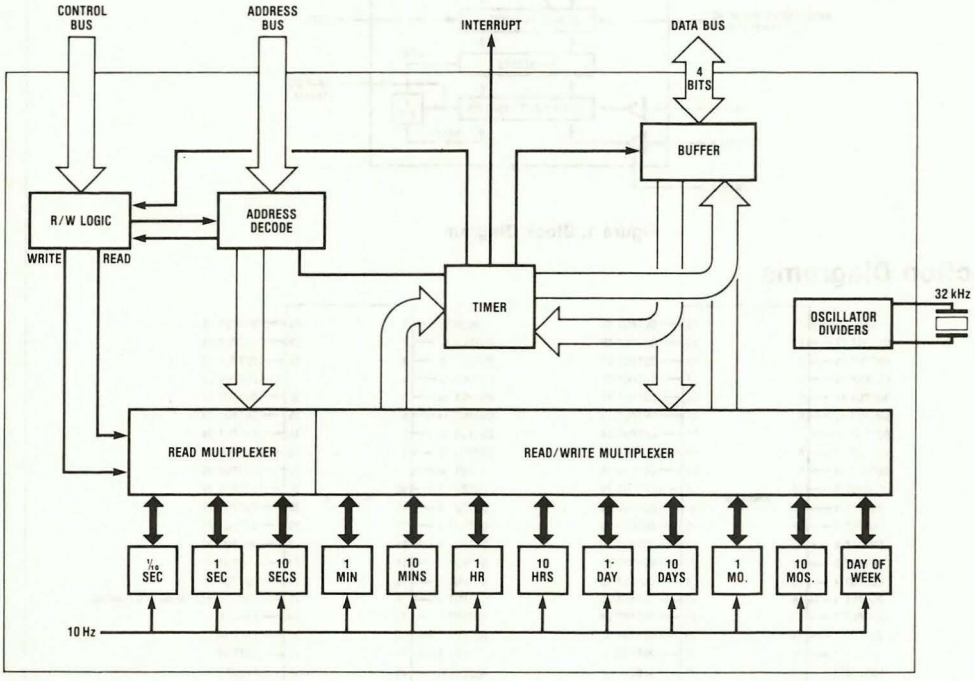

Figure 1. Block Diagram

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Circle DATA UPDATE No. 111333

National Semiconductor

April 1982
PRELIMINARY

MM58248, MM58241 High Voltage Display Drivers

General Description

The MM58248 series are monolithic MOS integrated circuits utilizing a combined CMOS/Bipolar process with both MOS and Junction F.E.T. devices. They are available in 40-pin dual-in-line packages, or as dice. Each output can source 1mA at 2V maximum output voltage, and also has an internal Junction F.E.T. to the display supply voltage which can be up to 60V. The possibility of brightness control is also provided.

- MICROWIRE™ compatible (MM58241)
- Simple to cascade (MM58241)
- Wide supply operation
- TTL compatible inputs
- Software compatible with NS display driver family
- Compatible with VF, high voltage LCD, and colloidal displays

Features

- Direct interface to 60V VF display
- Brightness and display blanking control input (MM58241)
- No resistors needed
- No load signal required (MM58248)

Applications

- COPS™ or microprocessor displays
- Instrumentation readouts
- Integrated dashboard displays
- Word processor text display

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Block Diagram

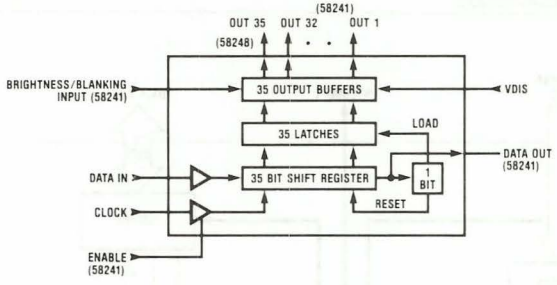

Figure 1. Block Diagram

Connection Diagrams

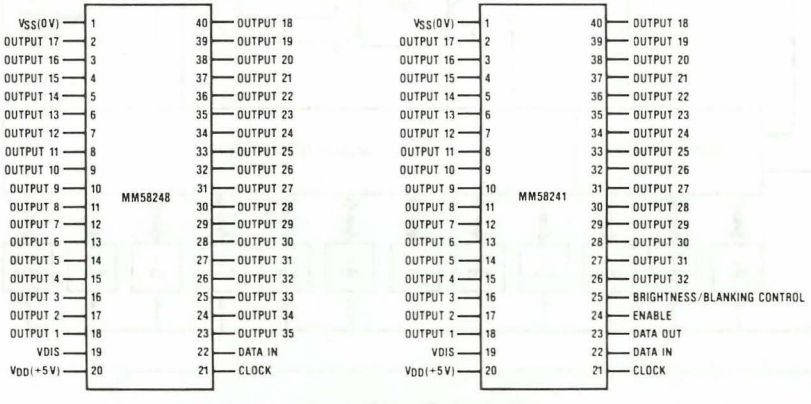

Figure 2.

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Circle DATA UPDATE No. 111394

National Semiconductor

April 1982
PRELIMINARY

MM58348, MM58341 High Voltage Display Drivers

General Description

The MM58348 series are monolithic MOS integrated circuits utilizing a combined CMOS/Bipolar process with both MOS and Junction F.E.T. devices. They are available in 40-pin molded dual-in-line packages or as dice. Each output can source 3mA at 1V maximum output voltage, and also has an internal Junction F.E.T. to the display supply voltage which can be up to 32V. The possibility of brightness control is also provided.

Features

- Direct interface to 32V VF display
- Brightness and display blanking control input (MM58341)
- No resistors needed
- No load signal required (MM58348)
- MICROWIRE™ compatible (MM58341)
- Simple to cascade (MM58341)
- Wide supply operation
- TTL compatible inputs
- Software compatible with NS display driver family
- Compatible with VF, high voltage LCD, and colloidal displays

Applications

- COPS™ or microprocessor displays
- Instrumentation readouts
- Integrated dashboard displays
- Word processor text display

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Block Diagram

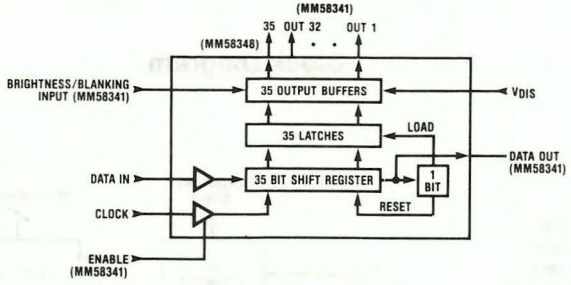

Figure 1. Block Diagram

Connection Diagrams

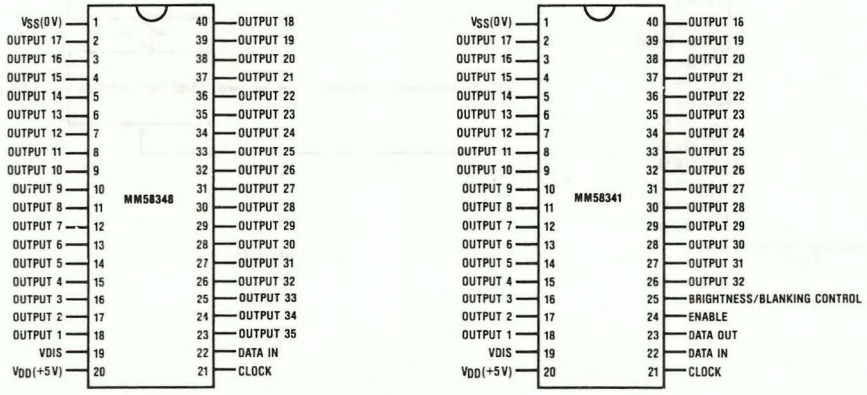

Figure 2.

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Circle DATA UPDATE No. 111428

National Semiconductor

PRELIMINARY
April 1982

MM58438 32-Bit LCD Display Driver

General Description

The MM58438 is a CMOS metal gate circuit which is capable of driving up to 32 LCD segments and is available in a 40-pin molded package. In addition, MM58438 dice is available for PCB module assembly systems. The circuit requires a minimum of interface between data source and display and can be cascaded where larger displays are required.

Features

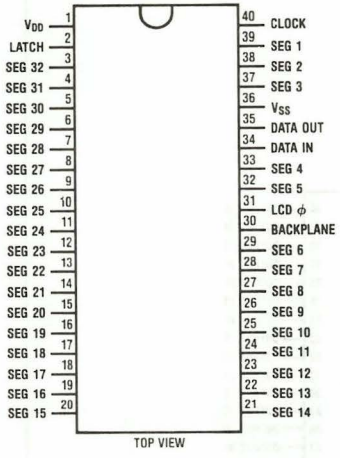
- Serial data input
- 32 segment outputs
- Cascaded operation capability
- Alphanumeric and bar graph capability
- TTL compatibility
- Non-multiplex display
- Compatible with HLCD 0438, HLCD.0438A
- Stable oscillator only requires one external component

Applications

- COPS™ or microprocessor displays
- Instrumentation readouts
- Digital clock, thermometer, counter, voltmeter displays
- Industrial control indicator
- Serial to parallel converter

Connection Diagram

Dual-In-Line Package



Block Diagram

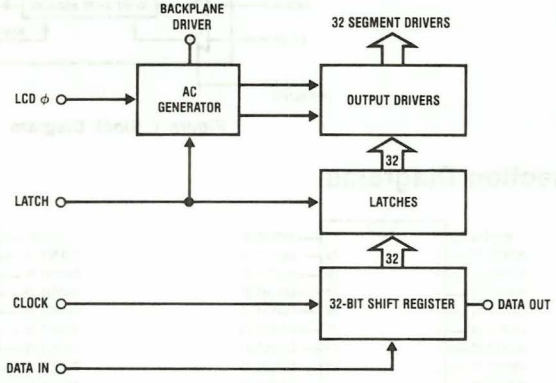


FIGURE 1

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Circle DATA UPDATE No. 111430

ADVANCED BIPOLAR LOGIC DATABOOK

DESCRIPTION

This is the Advanced Bipolar Logic Databook from National Semiconductor. The book contains information on the Advanced Schottky family, as well as the most up-to-date information available from National on the Advanced Low Power Schottky family.

Both of these advanced logic families are in their early production phases and will be continually expanded in future National Databook Publications.

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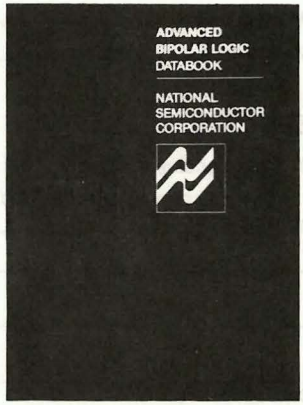

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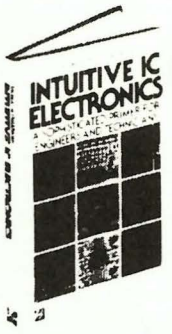

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National Semiconductor

PRELIMINARY
September 1982

MM54HC04/MM74HC04 Hex Inverter

General Description

This logic gate utilizes silicon gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

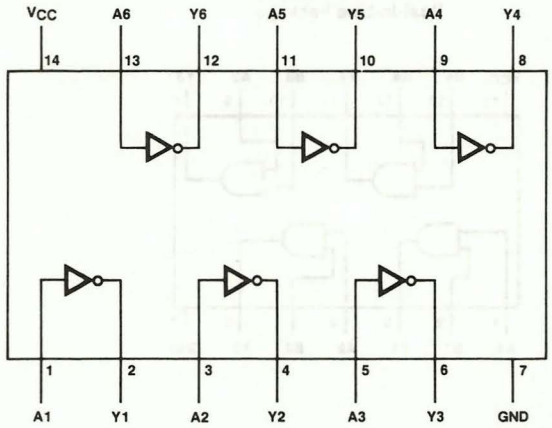
The MM54HC04/MM74HC04 is a triple buffered inverter. It has high noise immunity and the ability to drive 10 LS-TTL loads (8 LS-TTL loads for 54HC). The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8ns
- Fan out of 10 LS-TTL loads
- Quiescent power consumption: 10μW maximum at room temperature
- Typical input current: $10^{-5}\mu$A

Connection Diagram

MM54HC04/MM74HC04
Dual-In-Line Package



Logic Diagram

1 of 6 Inverters

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Circle DATA UPDATE No. 111604

National Semiconductor

August 1982

MM54HC08/MM74HC08 Quad 2-Input AND Gate

General Description

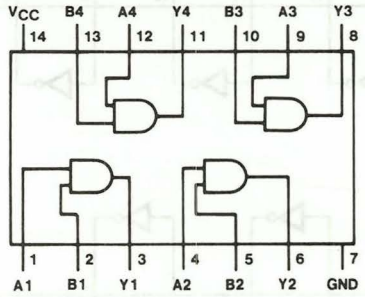
This AND gate utilizes silicon gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. The HC08 has buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads (8 LS-TTL loads for 54HC). The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 7ns (t_{PHL}), 12ns (t_{PLH})
- Fanout of 10 LS-TTL loads
- Quiescent power consumption: 10μW maximum at room temperature
- Typical input current: $10^{-5}\mu$A

Connection Diagram

MM54HC08/MM74HC08
Dual-In-Line Package



Y = AB

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Circle DATA UPDATE No. 111605

National Semiconductor

PRELIMINARY
September 1982

MM54HC11/MM74HC11 Triple 3-Input AND Gate

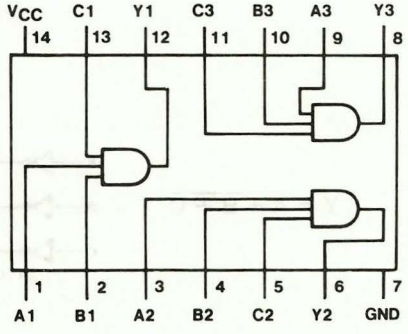
General Description

These AND gates utilize silicon gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads (8 LS-TTL loads for 54HC). The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

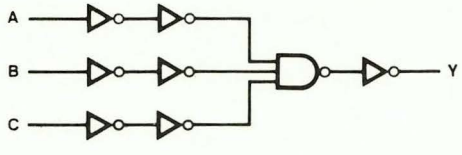
- Typical propagation delay: 12ns
- Wide power supply range: 2-6V
- Low quiescent current: 20μA maximum (74HC series)
- Low input current: 1μA maximum
- Fanout of 10 LS-TTL loads (74HC series)

Connection Diagram



MM54HC11/MM74HC11
Dual-In-Line Package

Logic Diagram



(1 OF 3 GATES)

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GL-B25M92/Printed in USA

Circle DATA UPDATE No. 111606

National Semiconductor

June 1982
PRELIMINARY

MM54HC27/MM74HC27 Triple 3-Input NOR Gate

General Description

This NOR gate utilizes silicon gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads (8 LS-TTL loads for the 54HC). The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

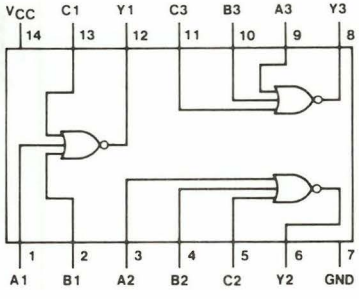
Features

- Typical Propagation Delay: 8 ns
- Wide Operating Supply Voltage Range: 2-6V
- Low Input Current: $< 1\mu A$
- Low Quiescent Supply Current: $40\mu A$ maximum (74HC series)
- Fanout of 10 LS-TTL Loads (74HC) or 8 LS-TTL Loads (54HC)

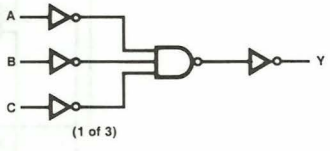
Connection and Logic Diagrams

MM54HC27/MM74HC27

Dual-In-Line Package



$$Y = \overline{A + B + C}$$



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September 1982

National Semiconductor

MM54HC75/MM74HC75
4 Bit Bistable Latch with Q and $\overline{Q}$ Output

General Description

This high speed 4-Bit Latch is fabricated with silicon gate CMOS technology. It possesses the high noise immunity and low power consumption normally associated with standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads (8 LS-TTL loads for 54HC).

This latch is ideally suited for use as temporary storage for binary information processing, input/output, and indicator units. Information present at the data (D) input is transferred to the Q output when the enable (G) is high. The Q output will follow the data input as long as the enable remains high. When the enable goes low, the information that was present at the data input at the time the transition occurred is retained at the Q output until the enable is permitted to go high again.

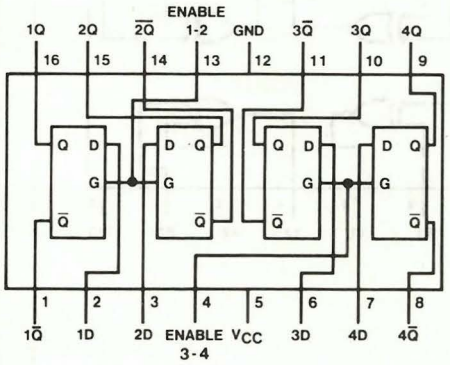
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 50MHz
- Typical propagation delay: 12ns
- Wide operating supply voltage range: 2-6V
- Low input current: $< 1\mu A$
- Low quiescent supply current: $80\mu A$ maximum (74HC series)
- Fanout of 10 LS-TTL loads (74HC) or 8 LS-TTL loads (54HC)

Connection and Logic Diagrams

MM54HC75/MM74HC75
Dual-in-Line Package

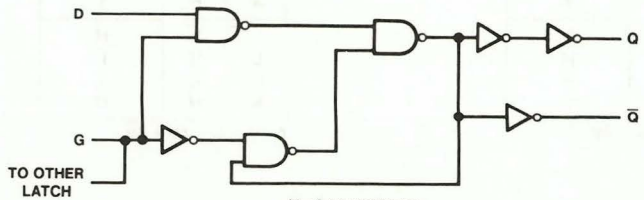


Truth Table

Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level; L = Low Level
X = Don't Care;
Q_0 = The level of Q before the transition of G

Logic Diagram



(1 of 4 LATCHES)

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GL-B25M92/Printed in USA

Circle DATA UPDATE No. 111608

National Semiconductor

PRELIMINARY
September 1982

MM54HC86/MM74HC86 Quad 2-Input Exclusive OR Gate
MM54HC266/MM74HC266 Quad 2-Input Exclusive NOR Gate

MM54HC86/MM74HC86 Quad 2-Input Exclusive OR Gate
MM54HC266/MM74HC266 Quad 2-Input Exclusive NOR Gate

General Description

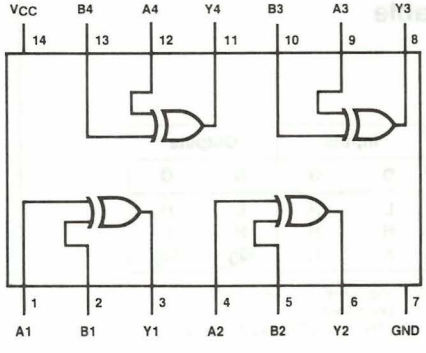
These EXCLUSIVE OR and EXCLUSIVE NOR gates utilize silicon gate CMOS technology to achieve operating speeds similar to equivalent LS-TTL gates while maintaining the low power consumption and high noise immunity characteristic of standard CMOS integrated circuits. Both gates are fully buffered and have a fanout of 10 LS-TTL loads (8 LS-TTL loads for 54HC). The MM54HC/74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

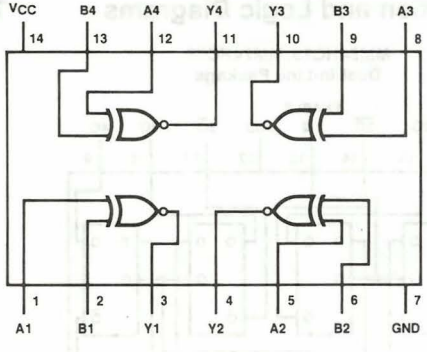
- Typical propagation delay: 9ns
- Wide operating voltage range: 2-6V
- Low input current: 1μA maximum
- Low quiescent current: 20μA maximum (74 series)
- Output drive capability: 10 LS-TTL loads (74HC series), 8 LS-TTL loads (54HC series)

Connection Diagrams

MM54HC86/MM74HC86
Dual-In-Line Package



MM54HC266/MM74HC266
Dual-In-Line Package



Truth Tables

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

$Y = A \oplus B = \overline{A}B + A\overline{B}$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

$Y = \overline{A \oplus B} = AB + \overline{A}\overline{B}$

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GL-B25M92/Printed in USA

Circle DATA UPDATE No. 111609

National Semiconductor

July 1982
PRELIMINARY

MM54HC139/MM74HC139 Dual 2-To-4 Line Decoder

General Description

This device is a high speed silicon gate CMOS decoder, and well suited to memory address decoding or data routing applications. It possesses the high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

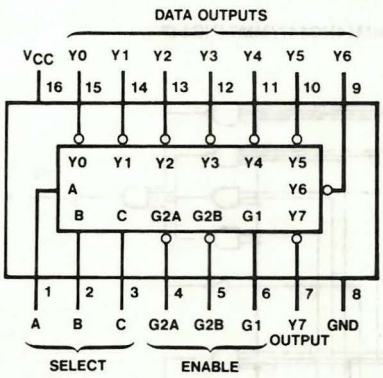
The MM54HC139/MM74HC139 contain two independent one-of-four decoders each with a single active low enable input (G1, or G2). Data on the select inputs (A1, and B1 or A2, and B2) cause one of the four normally high outputs to go low.

The decoder's outputs can drive 10 low power Schottky TTL equivalent loads (8 loads for 54HC), and are functionally as well as pin equivalent to the 54LS139/74LS139. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical Propagation Delays—
  Select to Output (4 delays): 20ns
  Select to Output (5 delays): 30ns
  Enable to Output: 20ns
- Low Power: 40μW Quiescent Supply Power
- Fanout of 10 LS-TTL devices (74HC)
- Input Current max 1μA, typical 10pA

Connection Diagram


DATA OUTPUTS
VCC Y0 Y1 Y2 Y3 Y4 Y5 Y6
16 15 14 13 12 11 10 9
Y0 Y1 Y2 Y3 Y4 Y5
A Y6
B C G2A G2B G1 Y7
1 2 3 4 5 6 7 8
A B C G2A G2B G1 Y7 GND
OUTPUT
SELECT
ENABLE

Truth Table

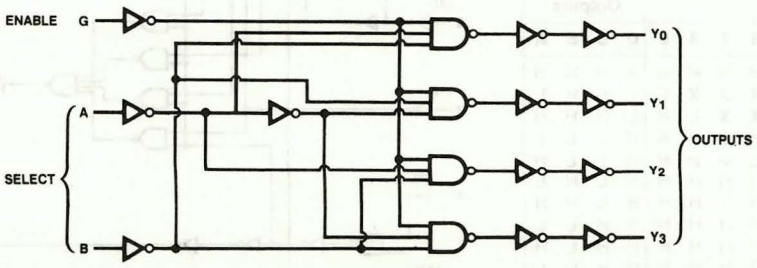
'HC139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

Logic Diagram

½ MM54HC139/MM74HC139



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GL-B25M72/Printed in U.S.A.

Circle DATA UPDATE No. 111612

National Semiconductor

PRELIMINARY
September 1982

MM54HC147/MM74HC147 10-to-4 Line Priority Encoder

General Description

This high speed 10-to-4 Line Priority Encoder is fabricated with silicon gate CMOS technology. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits. This device is fully buffered, giving it a fanout of 10 LS-TTL loads (8 LS-TTL loads for 54HC).

The MM54HC147/MM74HC147 features priority encoding of the inputs to ensure that only the highest order data line is encoded. Nine input lines are encoded to a four line BCD output. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All data inputs and outputs are active at the low logic level.

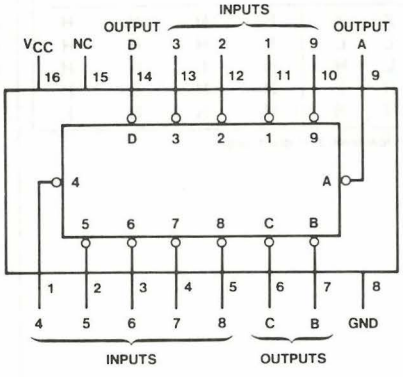
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent power consumption: 40μW maximum at 25°C
- High speed: 20ns propagation delay (typical)
- Very low input current: 10^{-5} μA typical
- Wide supply range: 2V to 6V

Connection Diagram

MM54HC147/MM74HC147
Dual-In-Line Package



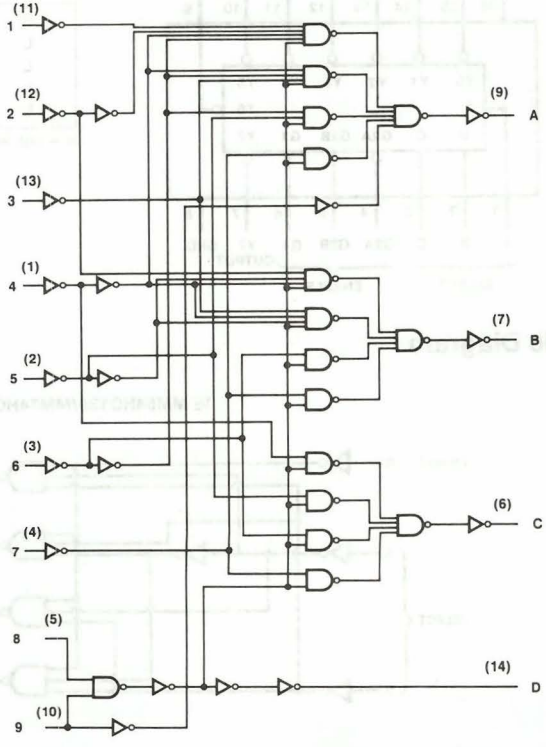
Truth Table

Inputs									Outputs			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Logic Level, L = Low Logic Level, X = Irrelevant

Logic Diagram

MM54HC147/MM74HC147



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GL-B25M92/Printed in USA

Circle DATA UPDATE No. 111611

July 1982

National Semiconductor

MM54HC151/MM74HC151 8-Channel Digital Multiplexer

General Description

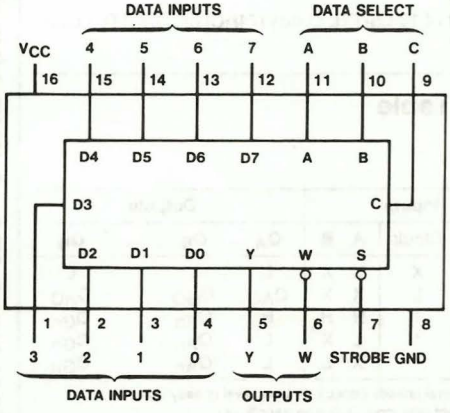
This high speed DIGITAL MULTIPLEXER is fabricated with the silicon gate CMOS technology. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads (8 LS-TTL loads for 54HC). The MM54HC151/MM74HC151 selects one of the 8 data sources, depending on the address presented on the A, B, and C inputs. It features both true (Y) and complement (W) outputs. The STROBE input must be at a low logic level to enable this multiplexer. A high logic level at the STROBE forces the W output high and the Y output low.

The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical Propagation Delay
  Data Select to Output Y: 26ns
- Wide Operating Supply Voltage Range: 2-6V
- Low Input Current: $<1\mu A$ Max
- Low Quiescent Supply Current: $80\mu A$ Max (74HC)
- High Output Drive Current: 4mA Min (74HC)

Connection Diagram

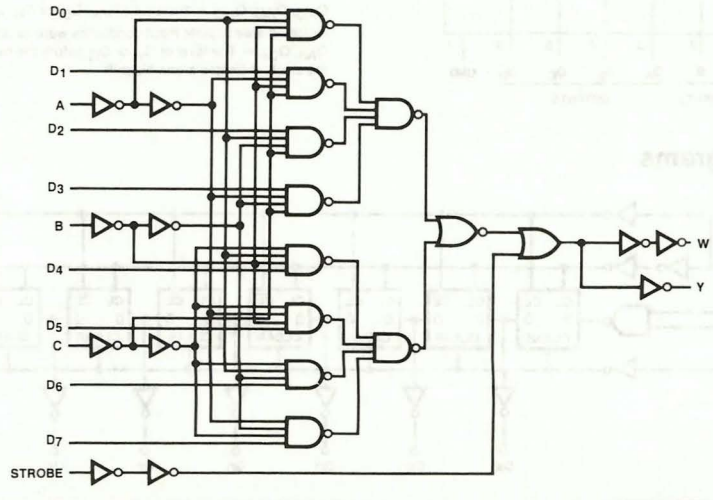

DATA INPUTS
DATA SELECT
VCC
4 5 6 7 A B C
16 15 14 13 12 11 10 9
D4 D5 D6 D7 A B
D3
C
D2 D1 D0 Y W S
1 2 3 4 5 6 7 8
3 2 1 0 Y W STROBE GND
DATA INPUTS
OUTPUTS

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care
D0, D1...D7 = the level of the respective D input

Logic Diagram



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GL/B30M072/Printed in U.S.A.

Circle DATA UPDATE No. 111613

National Semiconductor

June 1982
PRELIMINARY

MM54HC164/MM74HC164
8-Bit Serial-in/Parallel-out Shift Register

General Description

The MM54HC164/MM74HC164 is fabricated with high speed silicon gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8-BIT SHIFT REGISTER has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-BIT REGISTER during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

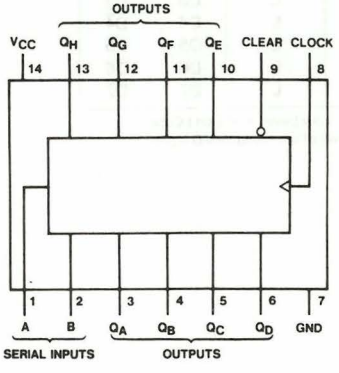
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical Operating Frequency: 50MHz
- Typical Propagation Delay: 19ns (Clock to Q)
- Wide Operating Supply Voltage Range: 2-6V
- Low Input Current: $< 1\mu A$
- Low Quiescent Supply Current: $80\mu A$ maximum (74HC Series)
- Fanout of 10 LS-TTL Loads (74HC) or 8 LS-TTL Loads (54HC)

Logic Diagram

Dual-in-Line Package
MM54HC164/MM74HC164

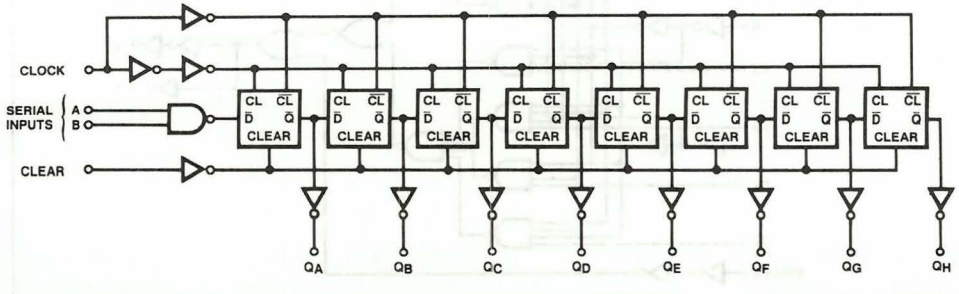


Truth Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{AO}	Q_{BO}		Q_{HO}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = High Level (steady state). L = Low Level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from low to high level.
Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagrams



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GL-B25M62/Printed in USA

Circle DATA UPDATE No. 111614

National Semiconductor

May 1982

MM54HC174/MM74HC174 Hex D Flip-Flops With Clear

General Description

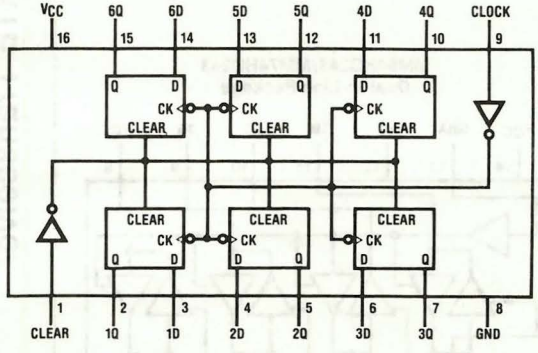
These edge triggered flip-flops utilize silicon gate CMOS circuitry to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 6 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the CLOCK input. The CLEAR input when low, sets all outputs to a low state.

Each output can drive 10 low power Schottky TTL equivalent loads (8 loads for 54HC). The MM54HC174/MM74HC174 is functionally as well as pin compatible to the 54LS174/74LS174. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

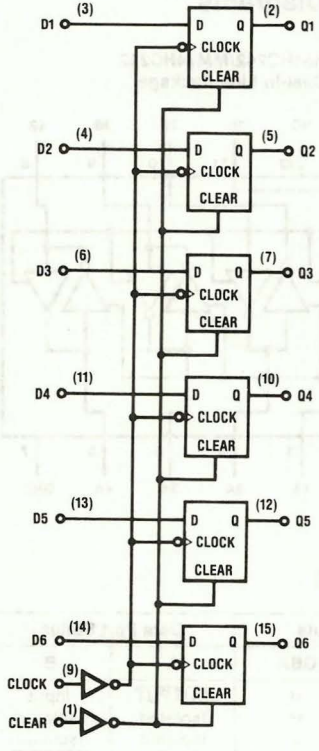
Features

- Typical propagation delay: 16ns
- Wide operating voltage range
- Low input current: 1μA maximum
- Low quiescient current 80μA (74 series)
- Output drive: 10 LSTTL loads (74 series)

Connection Diagram



Logic Diagram



Truth Table

(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High level (steady state)
L = Low level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.

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DA-B25M52/Printed in U.S.A.

Circle DATA UPDATE No. 111615

National Semiconductor

PRELIMINARY
September 1982

MM54HC242/MM74HC242 Inverting Quad TRI-STATE® Transceiver MM54HC243/MM74HC243 Quad TRI-STATE Transceiver

General Description

These silicon gate CMOS TRI-STATE bi-directional inverting and non-inverting buffers are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation when driving large bus capacitances. These circuits possess the low power dissipation and high noise immunity associated with CMOS circuits, but speeds comparable to low power Schottky TTL circuits. They can also drive 15 LS-TTL loads (10 loads for 54HC).

The MM54HC242/MM74HC242 is a non-inverting buffer and the MM54HC243/MM74HC243 is an inverting buffer. Each device has one active high enable (GBA), and one active low enable (GAB). GBA enables the A outputs and GAB enables the B outputs.

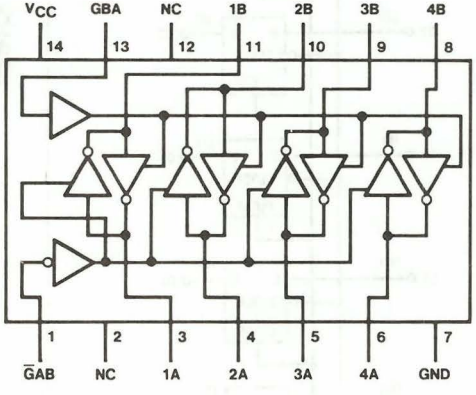
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

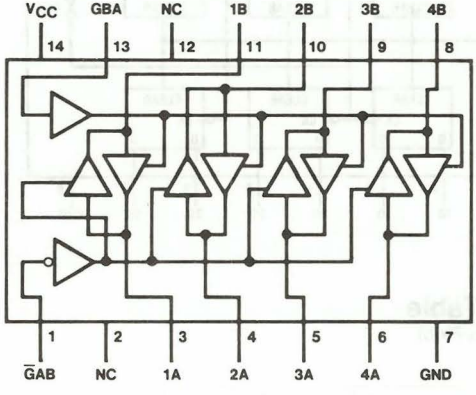
- Typical propagation delay: 12ns
- TRI-STATE outputs
- Two way asynchronous communication
- High output current: 6mA (74HC)
- Wide power supply range: 2-6V
- Low quiescent supply current: 80μA (74HC)

Connection Diagrams

MM54HC242/MM74HC242
Dual-In-Line Package



MM54HC243/MM74HC243
Dual-In-Line Package



Truth Tables

Control Inputs		Data Port Status	
$\overline{G}AB$	GBA	A	B
H	H	$\overline{OUTPUT}$	Input
L	H	Isolated	Isolated
H	L	Isolated	Isolated
L	L	Input	$\overline{OUTPUT}$

Control Inputs		Data Port Status	
$\overline{G}AB$	GBA	A	B
H	H	OUTPUT	Input
L	H	Isolated	Isolated
H	L	Isolated	Isolated
L	L	Input	OUTPUT

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GL-B25M92/Printed in USA

Circle DATA UPDATE No. 111617

MM54HC242/MM74HC242 Inverting Quad TRI-STATE Transceiver
MM54HC243/MM74HC243 Quad TRI-STATE Transceiver

July 1982

National Semiconductor

MM54HC251/MM74HC251 8-Channel TRI-STATE® Multiplexer

General Description

This 8-CHANNEL DIGITAL MULTIPLEXER with TRI-STATE outputs is fabricated with high speed silicon gate CMOS technology. Along with the high noise immunity and low power consumption of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads (8 LS-TTL loads for 54HC). The large output drive capability and TRI-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

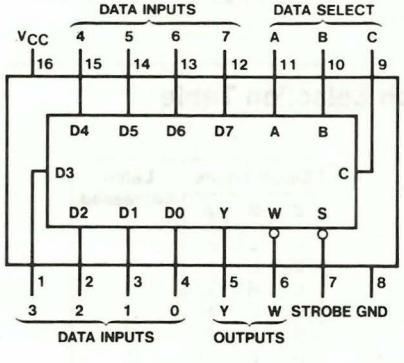
This multiplexer features both true (Y) and complement (W) outputs as well as a STROBE input. The STROBE must be at a low logic level to enable this device. When the STROBE input is high, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and W outputs. The 54HC/74HC logic family is speed, function, as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

TRI-STATE® is a Registered Trademark of National Semiconductor Corp.

Features

- Typical Propagation Delay
  Data Select to Y: 26ns
- Wide Supply Range: 2-6V
- Low Power Supply Quiescent Current: 80μA Maximum (74HC)
- TRI-STATE Outputs for Interface to Bus Oriented Systems

Connection Diagram

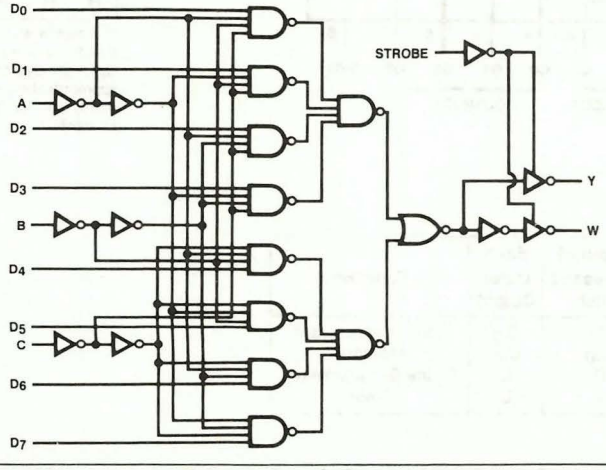

DATA INPUTS
DATA SELECT
VCC
4 5 6 7 A B C
16 15 14 13 12 11 10 9
D4 D5 D6 D7 A B
D3
C
D2 D1 D0 Y W S
1 2 3 4 5 6 7 8
3 2 1 0 Y W STROBE GND
DATA INPUTS
OUTPUTS

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1...D7 = the level of the respective D input

Logic Diagram



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GL/B30M072/Printed in U.S.A.

Circle DATA UPDATE No. 111620

National Semiconductor

PRELIMINARY
September 1982

MM54HC259/MM74HC259
8-Bit Addressable Latch/3-to-8 Line Decoder

General Description

This device utilizes silicon gate CMOS technology to implement an 8-bit addressable latch, designed for general purpose storage applications in digital systems.

The MM54HC259/MM74HC259 has a single data input (D), 8 latch outputs (Q1-Q8), 3 address inputs (A, B, and C), a common enable input (E), and a common CLEAR input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs. When ENABLE is taken low the data flows through to the addressed output. The data is stored when ENABLE transitions from low to high. All unaddressed latches will remain unaffected. With enable in the high state the device is deselected, and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the enable should be held high (inactive) while the address lines are changing.

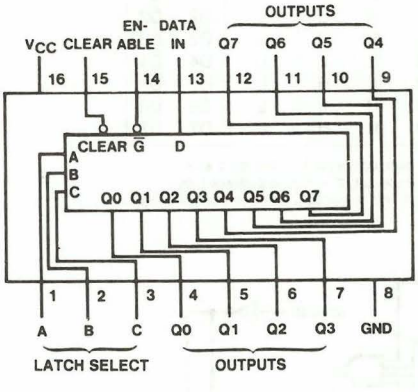
If enable is held high and CLEAR is taken low all eight latches are cleared to a low state. If enable is low all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to-8 line decoder.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 18ns
- Wide supply range: 2-6V
- Low input current: 1μA maximum
- Low quiescent supply current: 80μA maximum (74HC series)

Connection Diagram


OUTPUTS
EN- DATA
VCC CLEAR ABLE IN Q7 Q6 Q5 Q4
16 15 14 13 12 11 10 9
CLEAR G D
A
B
C
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
1 2 3 4 5 6 7 8
A B C Q0 Q1 Q2 Q3 GND
LATCH SELECT
OUTPUTS

Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = high level, L = low level
D = the level at the data input
Q_{i0} = the level of Q_i (i = 0, 1...7, as appropiate) before the indicated steady-state input conditions were established.

Truth Table

Inputs		Output of Addressed Latch	Each Other Output	Function
Clear	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

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GL-B25M92/Printed in USA

Circle DATA UPDATE No. 111622

National Semiconductor

PRELIMINARY
September 1982

MM54HC390/MM74HC390 Dual 4-Bit Decade Counter
MM54HC393/MM74HC393 Dual 4-Bit Binary Counter

MM54HC390/MM74HC390 Dual 4-Bit Decade Counter
MM54HC393/MM74HC393 Dual 4-Bit Binary Counter

General Description

These high speed silicon gate CMOS counter circuits contain independent ripple carry counters. The MM54HC390/MM74HC390 incorporate dual decade counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual biquinary, or various combinations up to a single divide-by-100 counter. The MM54HC393/MM74HC393 contain two 4-bit ripple carry binary counters, which can be cascaded to create a single divide-by-256 counter.

Each of the two 4-bit counters is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

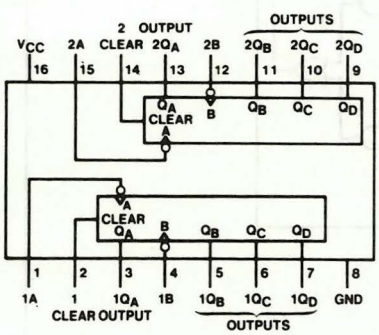
Each of the counters outputs can drive 10 low power Schottky TTL equivalent loads (8 loads for 54HC). These counters are functionally as well as pin equivalent to the 54LS390/74LS390 and the 54LS393/74LS393, respectively. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

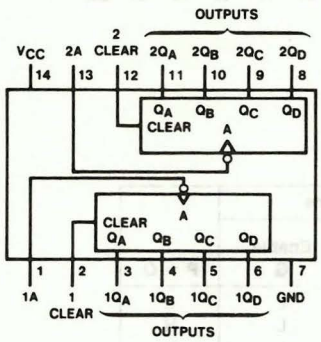
- Typical operating frequency: 50MHz
- Typical propagation delay: 13ns (Ck to Q_A)
- Wide operating supply voltage range: 2-6V
- Low input current: $< 1\mu A$
- Low quiescent supply current: $80\mu A$ maximum (74HC Series)
- Fanout of 10 LS-TTL loads (74HC) or 8 LS-TTL loads (54HC)

Connection Diagrams

MM54HC390/MM74HC390
Dual-In-Line Package


2 OUTPUT
OUTPUTS
VCC 2A CLEAR 2QA 2B 2QB 2QC 2QD
16 15 14 13 12 11 10 9
QA CLEAR B QB QC QD
A
CLEAR QA B QB QC QD
1 2 3 4 5 6 7 8
1A 1 CLEAR 1QA OUTPUT 1B 1QB 1QC 1QD GND
OUTPUTS

MM54HC393/MM74HC393
Dual-In-Line Package


OUTPUTS
2
VCC 2A CLEAR 2QA 2QB 2QC 2QD
14 13 12 11 10 9 8
QA QB QC QD CLEAR A
CLEAR QA QB QC QD
1 2 3 4 5 6 7
1A 1 CLEAR 1QA 1QB 1QC 1QD GND
OUTPUTS

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Circle DATA UPDATE No. 111624

National Semiconductor

PRELIMINARY
September 1982

MM54HC688/MM74HC688
8-Bit Magnitude Comparator (Equality Detector)

General Description

This circuit is a high speed equality detector that compares bit for bit two 8-bit words and indicates whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

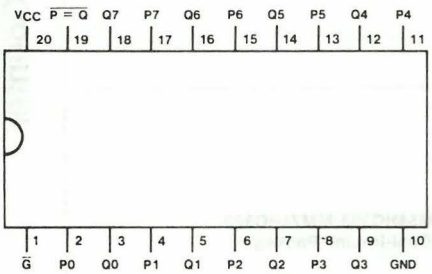
The comparator's output can drive 10 low power Schottky equivalent loads (8 for 54HC). This comparator is functionally and pin compatible to the 54LS688/74LS688. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

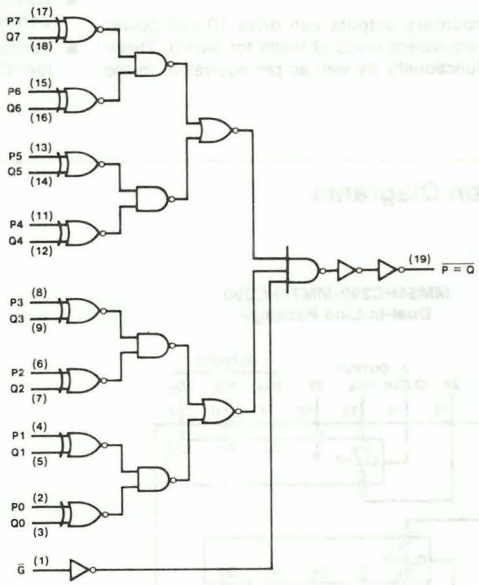
Features

- Typical propagation delay: 20ns
- Wide power supply range: 2-6V
- Low quiescent supply current: 80μA (74 series)
- Large output current: 4mA (74 series)

Connection and Logic Diagrams

MM54HC688/MM74HC688
Dual-In-Line Package





Truth Table

Inputs		
Data P,Q	Enable $\overline{G}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

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GL-B25M92/Printed in USA

Circle DATA UPDATE No. 111632

National Semiconductor

September 1982

MM54HCU04/MM74HCU04 Hex Inverter

General Description

This logic gate utilizes silicon gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

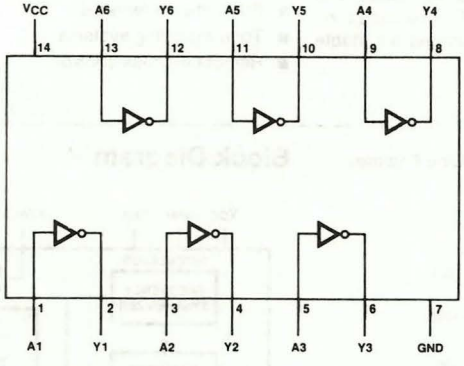
The MM54HCU04/MM74HCU04 is an unbuffered inverter. It has high noise immunity and the ability to drive 15 LS-TTL loads (12 LS-TTL loads for 54HCU). The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

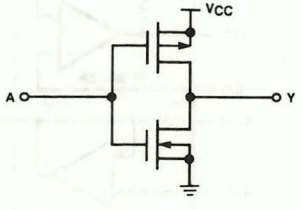
- Typical propagation delay: 7ns
- Fan out of 15 LS-TTL loads
- Quiescent power consumption: 10μW maximum at room temperature
- Typical input current: $10^{-5}\mu$A

Connection Diagram

MM54HCU04/MM74HCU04
Dual-In-Line Package



Schematic Diagram



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Circle DATA UPDATE No. 111645

National Semiconductor

PRELIMINARY
September 1982

MM74HC942 300 Baud Modem*

General Description

The MM74HC942 is a full duplex low speed modem. It provides a 300 baud bidirectional serial interface for data communication over telephone lines and other narrow bandwidth channels. It is Bell 103 compatible.

The device is manufactured on National's P^2 CMOS™ process. Switched capacitor techniques are used to perform analog signal processing.

MODULATOR SECTION

The modulator contains a frequency synthesizer and a sine wave synthesizer. It produces a phase coherent frequency shift keyed (FSK) output.

LINE DRIVER AND HYBRID SECTION

The line driver and hybrid are designed to facilitate connection to a 600 Ω phone line. They can perform two to four wire conversion and drive the line at 0 dBm.

DEMODULATOR SECTION

The demodulator incorporates anti-aliasing filters, a receive filter, limiter, discriminator, and carrier detect circuit. The nine pole receive filter provides 60 dB of transmitted tone rejection. The discriminator is fully balanced for stable operation.

P^2 CMOS™ is a trademark of National Semiconductor Corp.

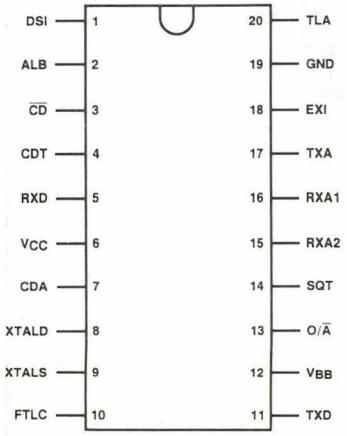
Features

- Drives 600 Ω at 0 dBm
- All filters on chip
- Transmit level adjustment compatible with universal service order code
- TTL and CMOS compatible logic
- All inputs protected against static damage
- ±5V supplies
- Low power consumption
- Full duplex answer or originate operation
- Analog loopback for self test
- Power down mode

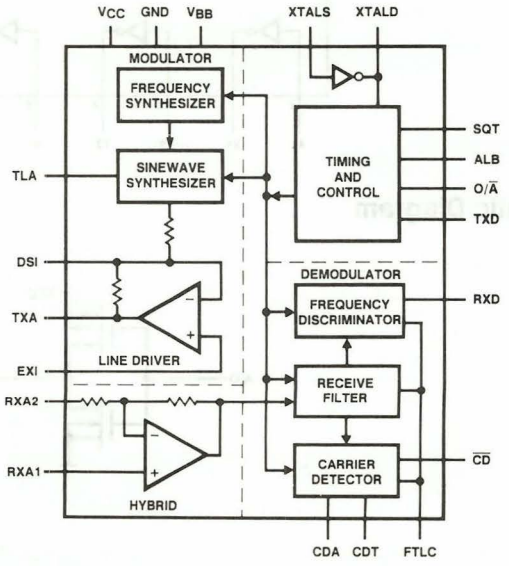
Applications

- Built-in low speed modems
- Remote data collection
- Radio telemetry
- Credit verification
- Stand-alone modems
- Point-of-sale terminals
- Tone signalling systems
- Remote process control

Connection Diagram Dual-in-Line Package



Block Diagram



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GL-B25M92/Printed in U.S.A.

Circle DATA UPDATE No. 111770

National Semiconductor

PRELIMINARY
May 1982

NMC27C32 32,768-Bit (4096 × 8) UV Erasable CMOS PROM

Parameter/Part Number	NMC27C32Q-35	NMC27C32Q-45	NMC27C32Q-55	NMC27C32Q-65
Access Time (ns)	350	450	550	650
Active Current (mA)	5	5	5	5
Standby Current (mA)	0.1	0.1	0.1	0.1

General Description

The NMC27C32 is a high speed 32k UV erasable and electrically reprogrammable CMOS EPROM ideally suited for applications where fast turn-around, pattern experimentation and low power consumption are important requirements.

The NMC27C32 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

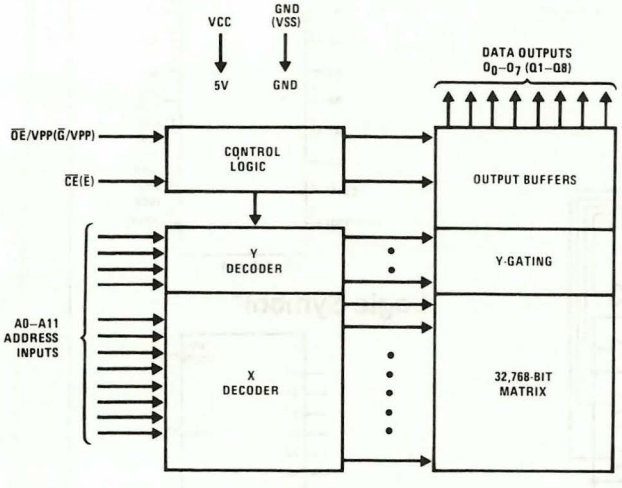
This EPROM is fabricated with the reliable, high volume, time proven, P²CMOS™ silicon gate technology.

P²CMOS™ and NSC800™ are trademarks of National Semiconductor Corp.
TRI-STATE® is a registered trademark of National Semiconductor Corp.

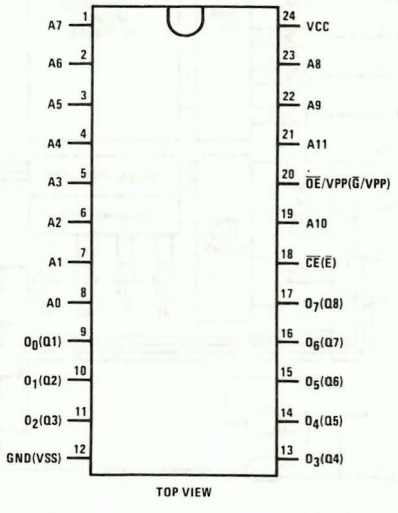
Features

- CMOS power consumption
  - 53 mW max active
  - 5.3 mW max standby
- Performance compatible to NSC800™ CMOS microprocessor and NMC6732 synchronous CMOS EPROM
- 4096 × 8 organization
- Pin compatible to 2732
- Access time down to 350 ns
- Single 5V power supply
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams*



Dual-In-Line Package



TOP VIEW

Modes*

Mode	Pin Name/Number			
	CE (E) 18	OE/VPP (G/VPP) 20	VCC 24	Outputs 9-11, 13-17
Read	VIL	VIL	5V	DOUT
Standby	VIH	Don't Care	5V	Hi-Z
Program	VIL	25V	5V	DIN
Program Verify	VIL	VIL	5V	DOUT
Program Inhibit	VIH	25V	5V	Hi-Z

Pin Names*

CE (E)	Chip Enable
OE (G)	Output Enable
A0-A11	Address Inputs
O0-O7 (Q1-Q8)	Data Outputs
VPP	Program Power 25V
VCC	Power 5V
GND (VSS)	Ground

*Symbols in parentheses are proposed industry standard.

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Circle DATA UPDATE No. 112261

NMC27C32 32,768-Bit (4096 × 8) UV Erasable CMOS PROM

National Semiconductor

August 1982

NMC2114A 1024 x 4 Static RAM

Maximum Access/Current	NMC2114A-1L	NMC2114A-2L	NMC2114A-3L	NMC2114A-4L	NMC2114A-4	NMC2114A-5
Access (t_{AA}—ns)	100	120	150	200	200	250
Active Current (ICC—mA)	40	40	40	40	70	70

General Description

The NMC2114A family of 1024-word by 4-bit static random access memories is fabricated using the XMOS II™ N-channel silicon-gate technology, incorporating poly-load resistors and two poly-silicon layers. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided. The separate chip select input ($\overline{CS}$) allows easy memory expansion by OR-tying individual devices to a data bus.

The NMC2114A is designed for memory applications where the high performance and high reliability of XMOS II, low cost and simple interfacing are important design objectives.

Features

- High performance replacement for industry standard MM2114
- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—220 mW maximum
- High speed—down to 100 ns access time
- TRI-STATE® output for bus interface
- Common data in and data out pins
- Single 5V ± 10% supply
- Standard 18-pin dual-in-line package

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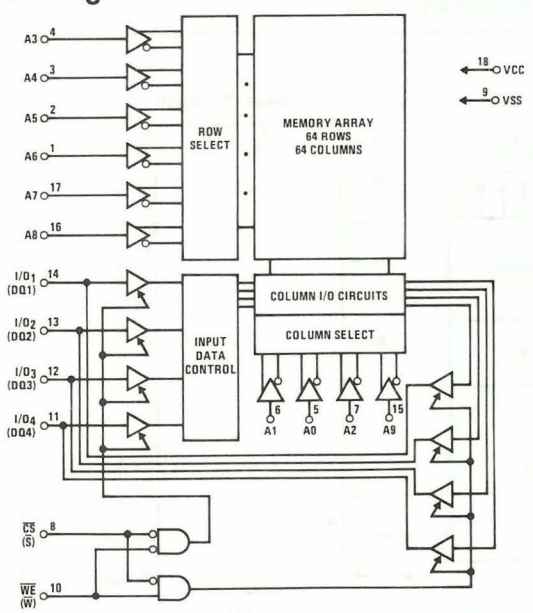
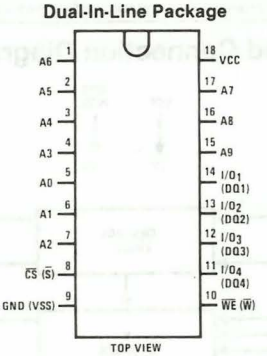
TRI-STATE® is a registered trademark of National Semiconductor Corp.

Block Diagram*



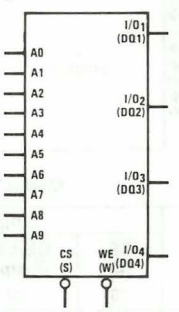
Connection Diagram*

Dual-In-Line Package



TOP VIEW

Logic Symbol*



Truth Table*

$\overline{CS}$ ($\overline{S}$)	$\overline{WE}$ ($\overline{W}$)	I/O (DQ)	Mode
H	X	Hi-Z	Not selected
L	L	H	Write 1
L	L	L	Write 0
L	H	DOUT	Read

X = don't care

*Symbols in parentheses are proposed industry standard

Pin Names*

A0-A9	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS}$ ($\overline{S}$)	Chip Select
I/O_1-I/O_4 (DQ1-DQ4)	Data Input/Output
VCC	Power (5V)
GND (VSS)	Ground

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IM-B25M82/Printed in U.S.A.

Circle DATA UPDATE No. 112229

National Semiconductor

PRELIMINARY
April 1982

NMC2816 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC2816-25	NMC2816-35	NMC2816-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	110	110	110
Max Standby Current (mA)	50	50	50

General Description

The NMC2816 is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC2816 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC2816 is deselected when pin 18 is high and is automatically placed in the standby mode. This mode provides a 52% reduction in power with no increase in access time. The NMC2816 also has an output enable control to eliminate bus contention in a system environment.

The NMC2816 can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array erased in a chip erase mode. Byte erase mode is identical to byte write mode, with all data inputs at logic ones (TTL high).

Features

- 2048 x 8 organization
- Fully static
- Reliable floating gate technology
- Very fast access time
  - 250 ns max (NMC2816-25)
  - 350 ns max (NMC2816-35)
  - 450 ns max (NMC2816-45)
- Single byte erase/write capability
- 10 ms byte erase/write time
- Chip erase time of 10 ms
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Low power dissipation
  - 610 mW max (active power ICC + IPP)
  - 295 mW max (standby power ICC + IPP)

Block and Connection Diagrams

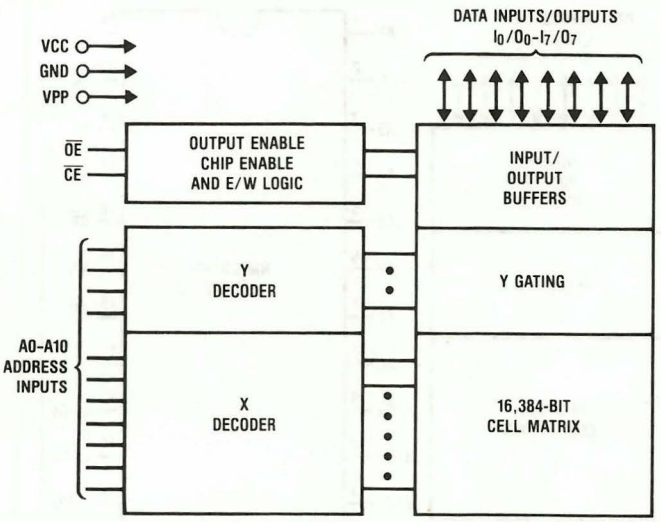
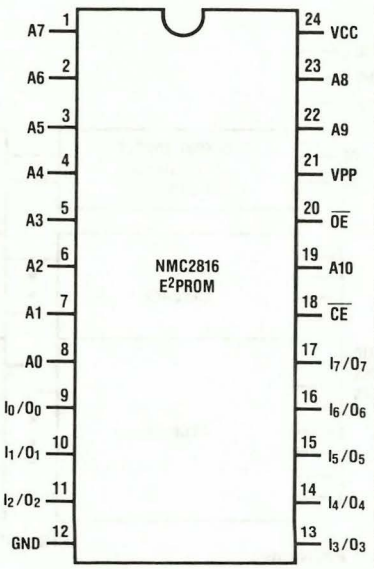


FIGURE 1

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

Dual-In-Line Package



TOP VIEW

FIGURE 2

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Circle DATA UPDATE No. 112234

National Semiconductor

PRELIMINARY
April 1982

NMC2816M 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC2816M-25	NMC2816M-35	NMC2816M-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	140	140	140
Max Standby Current (mA)	60	60	60

General Description

The NMC2816M is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC2816M makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC2816M is deselected when pin 18 is high and is automatically placed in the standby mode. This mode provides a 55% reduction in power with no increase in access time. The NMC2816M also has an output enable control to eliminate bus contention in a system environment.

The NMC2816M can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array erased in a chip erase mode. Byte erase mode is identical to byte write mode, with all data inputs at logic ones (TTL high).

Features

- 2048 x 8 organization
- Fully static
- Reliable floating gate technology
- Very fast access time
  - 250 ns max (NMC2816M-25)
  - 350 ns max (NMC2816M-35)
  - 450 ns max (NMC2816M-45)
- Single byte erase/write capability
- 10 ms byte erase/write time
- Chip erase time of 10 ms
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Low power dissipation
  - 800 mW max (active power ICC + IPP)
  - 360 mW max (standby power ICC + IPP)

Block and Connection Diagrams

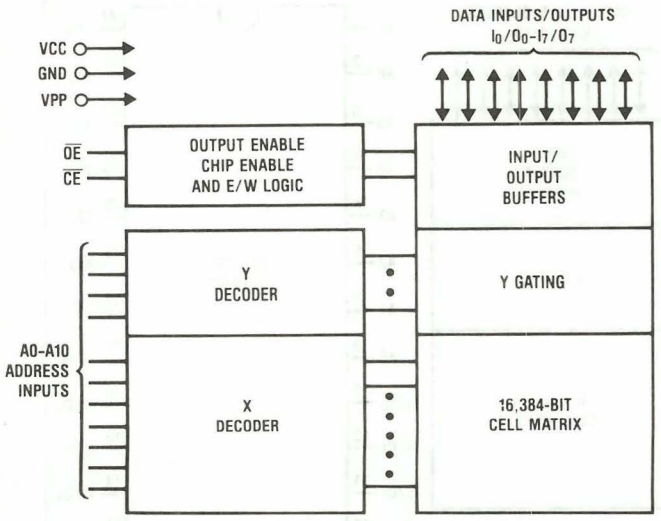
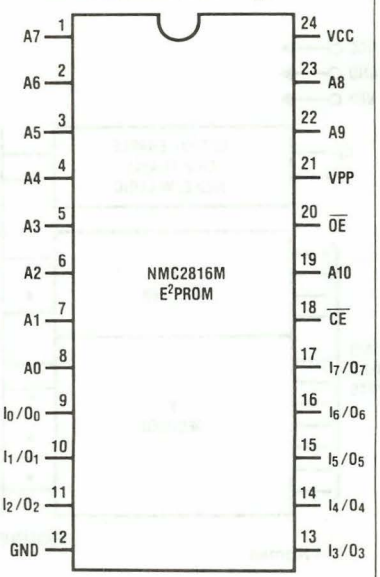


FIGURE 1

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

Dual-In-Line Package



TOP VIEW

FIGURE 2

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IM-B25M42/Printed in U.S.A.

Circle DATA UPDATE No. 112262

NMC2816M 16k (2k x 8) Electrically Erasable PROM

National Semiconductor

PRELIMINARY
May 1982

NMC6716 16,384-Bit (2048 × 8) UV Erasable CMOS PROM

Parameter/Part Number	NMC6716-45	NMC6716-55	NMC6716-65
Access Time (ns)	450	550	650
Active Current (mA)	5	5	5
Standby Current (mA)	0.1	0.1	0.1

General Description

The NMC6716 is a synchronous high speed 16k UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around, pattern experimentation and low power consumption are important requirements.

The NMC6716 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, P²CMOS™ silicon gate technology.

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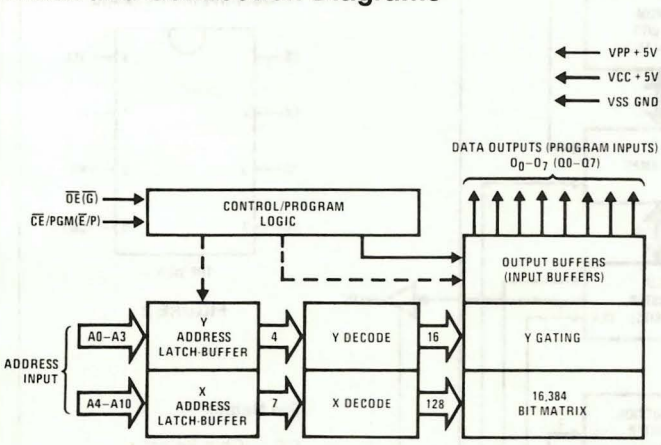
TRI-STATE® is a registered trademark of National Semiconductor Corp.

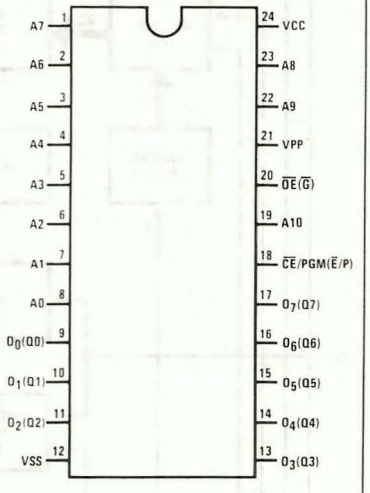
Features

- On-chip address registers (latches)
- CMOS power consumption
  - 53 mW max active
  - 5.3 mW max standby
- Performance compatible to NSC800™ CMOS microprocessor and NMC27C16 asynchronous CMOS EPROM
- 2048 × 8 organization
- Low power during programming
- High speed—down to 450 ns access time
- Single 5V power supply
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams*



Dual-In-Line Package



TOP VIEW

Pin Connection During Read or Program

Mode	Pin Name/Number				
	CE/PGM (E/P) 18	OE (G) 20	VPP 21	VCC 24	Outputs 9-11, 13-17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

Pin Names

A0–A10	Address Inputs
O_0–O_7(Q0–Q7)	Data Outputs
CE/PGM(E/P)	Chip Enable/Program
OE(G)	Output Enable
VPP	Read 5V, Program 25V
VCC	Power 5V
VSS	Ground

* Symbols in parentheses are proposed industry standard.

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IM-B25M52/Printed in U.S.A.

Circle DATA UPDATE No. 112255

National Semiconductor

PRELIMINARY
August 1982

NMC9306/COP494 256-Bit Serial Electrically Erasable Programmable Memory

General Description

The NMC9306/COP494 is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each word can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306/COP494 has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16 x 16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams

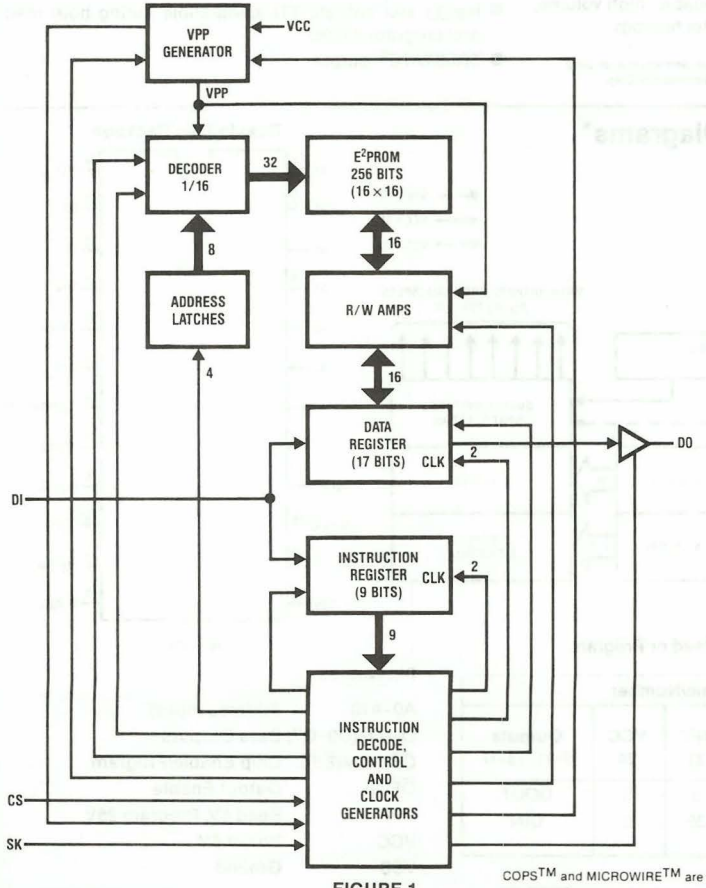
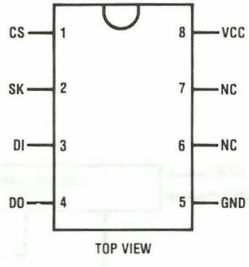


FIGURE 1

Dual-In-Line Package



TOP VIEW

FIGURE 2

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VCC	Power Supply
GND	Ground

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IM-B25M82/Printed in U.S.A.

Circle DATA UPDATE No. 112270

National Semiconductor

PRELIMINARY
April 1982

NMC9708 8k (1k × 8) Electrically Erasable PROM

Max Access/Current	NMC9708
Max Access Time (ns)	450
Max Active Current (mA)	110
Max Standby Current (mA)	50

General Description

The NMC9708 is an 8,192-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC9708 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The NMC9708 is pin and functionally compatible with the NMC2816 E^2PROM, with the added system feature of erasing/writing with a 5V TTL pulse on chip enable ($\overline{CE}$), while the VPP is held at 21V. The erase/write cycle is very similar to the industry standard 2716 EPROM programming cycle.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC9708 is deselected when $\overline{CE}$ input is high and is automatically placed in the standby mode. This mode provides a 52% reduction in power with no increase in access time. The NMC9708 also has an output enable control to eliminate bus contention in a system environment.

The NMC9708 can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array can be erased with a single programming pulse in the chip erase mode. Byte erase is identical to byte write, with all inputs at logic one (TTL high).

Features

- Erase/write with a 5V TTL pulse or a 21V pulse
- No rise time restriction on erase/write pulse
- 1024 × 8 organization
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Single byte erase/write capability
- 10 ms byte erase/write time
- 10 ms chip erase mode
- Low power dissipation
  610 mW max (active power ICC + IPP)
  295 mW max (standby power ICC + IPP)

Block and Connection Diagrams

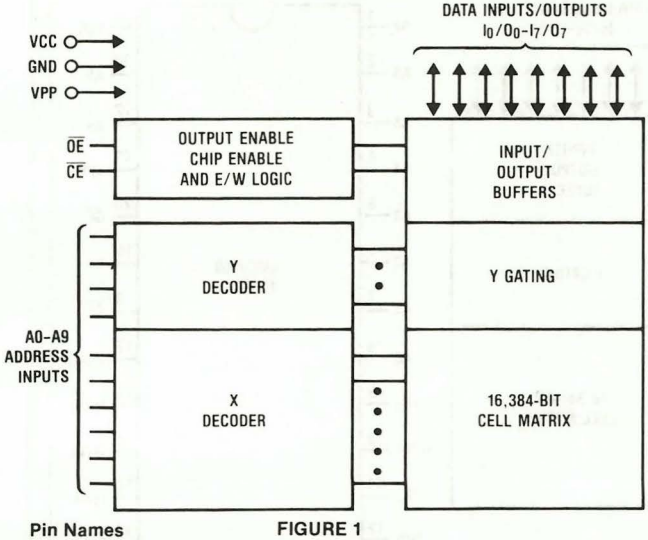
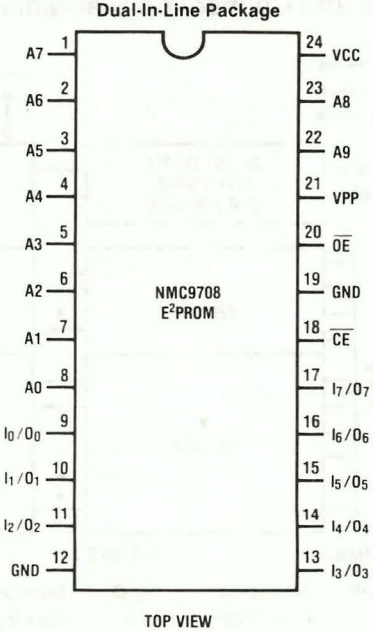


FIGURE 1



TOP VIEW

FIGURE 2

Pin Names

A0–A9	Addresses	O_0–O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0–I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

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IM-B25M42/Printed in U.S.A.

Circle DATA UPDATE No. 112263

National Semiconductor

PRELIMINARY
April 1982

NMC9709 8k (1k x 8) Electrically Erasable PROM

Max Access/Current	NMC9709
Max Access Time (ns)	450
Max Active Current (mA)	110
Max Standby Current (mA)	50

General Description

The NMC9709 is an 8,192-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC9709 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The NMC9709 is pin and functionally compatible with the NMC2816 E^2PROM, with the added system feature of erasing/writing with a 5V TTL pulse on chip enable ($\overline{CE}$), while the VPP is held at 21V. The erase/write cycle is very similar to the industry standard 2716 EPROM programming cycle.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

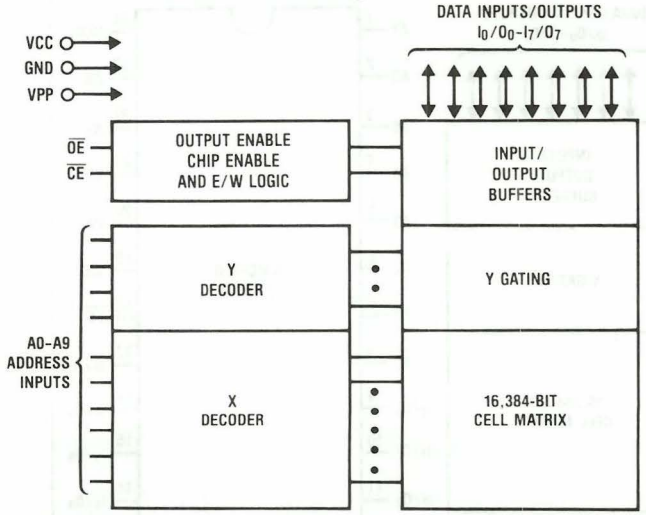
The NMC9709 is deselected when $\overline{CE}$ input is high and is automatically placed in the standby mode. This mode provides a 52% reduction in power with no increase in access time. The NMC9709 also has an output enable control to eliminate bus contention in a system environment.

The NMC9709 can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array can be erased with a single programming pulse in the chip erase mode. Byte erase is identical to byte write, with all inputs at logic one (TTL high).

Features

- Erase/write with a 5V TTL pulse or a 21V pulse
- No rise time restriction on erase/write pulse
- 1024 x 8 organization
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Single byte erase/write capability
- 10 ms byte erase/write time
- 10 ms chip erase mode
- Low power dissipation
  610 mW max (active power ICC + IPP)
  295 mW max (standby power ICC + IPP)

Block and Connection Diagrams

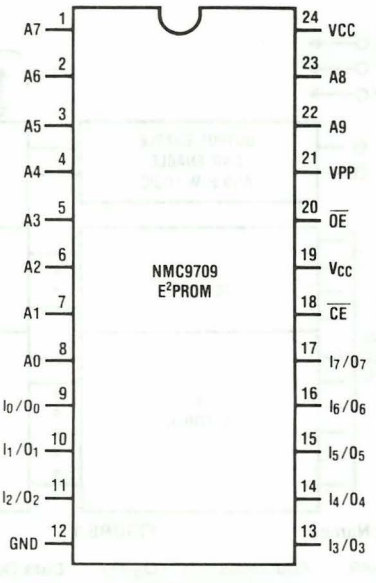


Pin Names

A0-A9	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

FIGURE 1

Dual-In-Line Package



TOP VIEW

FIGURE 2

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IM-B25M42/Printed in U.S.A.

Circle DATA UPDATE No. 112264

NMC9709 8k (1k x 8) Electrically Erasable PROM

National Semiconductor

PRELIMINARY
April 1982

NMC9716 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC9716-25	NMC9716-35	NMC9716-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	110	110	110
Max Standby Current (mA)	50	50	50

General Description

The NMC9716 is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC9716 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The NMC9716 is pin and functionally compatible with the NMC2816 E^2PROM, with the added system feature of erasing/writing with a 5V TTL pulse on chip enable ($\overline{CE}$), while the VPP is held at 21V. The erase/write cycle is very similar to the industry standard 2716 EPROM programming cycle.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC9716 is deselected when $\overline{CE}$ input is high and is automatically placed in the standby mode. This mode provides a 52% reduction in power with no increase in access time. The NMC9716 also has an output enable control to eliminate bus contention in a system environment.

The NMC9716 can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array can be erased with a single programming pulse in the chip erase mode. Byte erase is identical to byte write, with all inputs at logic one (TTL high).

Features

- Erase/write with a 5V TTL pulse or a 21V pulse
- Pin and functionally compatible with the NMC2816
- No rise time restriction on erase/write pulse
- 2048 x 8 organization
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Single byte erase/write capability
- 10 ms byte erase/write time
- 10 ms chip erase mode
- Low power dissipation
  610 mW max (active power ICC + IPP)
  295 mW max (standby power ICC + IPP)

Block and Connection Diagrams

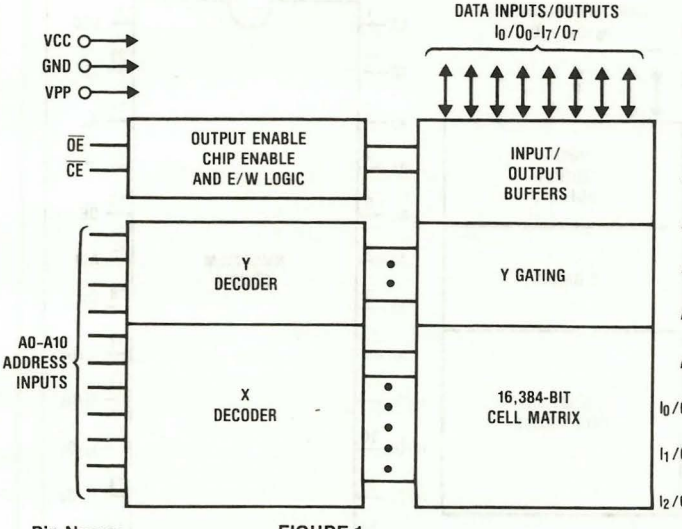
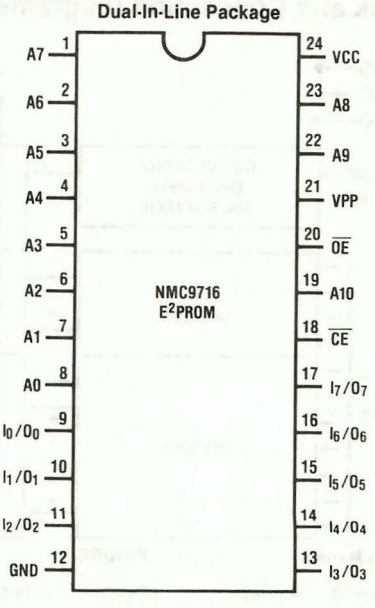


FIGURE 1



TOP VIEW

FIGURE 2

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

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IM-B25M42/Printed in U.S.A.

Circle DATA UPDATE No. 112265

National Semiconductor

PRELIMINARY
April 1982

NMC9716M 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC9716M-25	NMC9716M-35	NMC9716M-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	140	140	140
Max Standby Current (mA)	60	60	60

General Description

The NMC9716M is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC9716M makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The NMC9716M is pin and functionally compatible with the NMC2816M E^2PROM, with the added system feature of erasing/writing with a 5V TTL pulse on chip enable ($\overline{CE}$), while the VPP is held at 21V. The erase/write cycle is very similar to the industry standard 2716 EPROM programming cycle.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC9716M is deselected when $\overline{CE}$ input is high and is automatically placed in the standby mode. This mode provides a 55% reduction in power with no increase in access time. The NMC9716M also has an output enable control to eliminate bus contention in a system environment.

The NMC9716M can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array can be erased with a single programming pulse in the chip erase mode. Byte erase is identical to byte write, with all inputs at logic one (TTL high).

Features

- Erase/write with a 5V TTL pulse or a 21V pulse
- Pin and functionally compatible with the NMC2816M
- No rise time restriction on erase/write pulse
- 2048 x 8 organization
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Single byte erase/write capability
- 10 ms byte erase/write time
- 10 ms chip erase mode
- Low power dissipation
  800 mW max (active power ICC + IPP)
  360 mW max (standby power ICC + IPP)

Block and Connection Diagrams

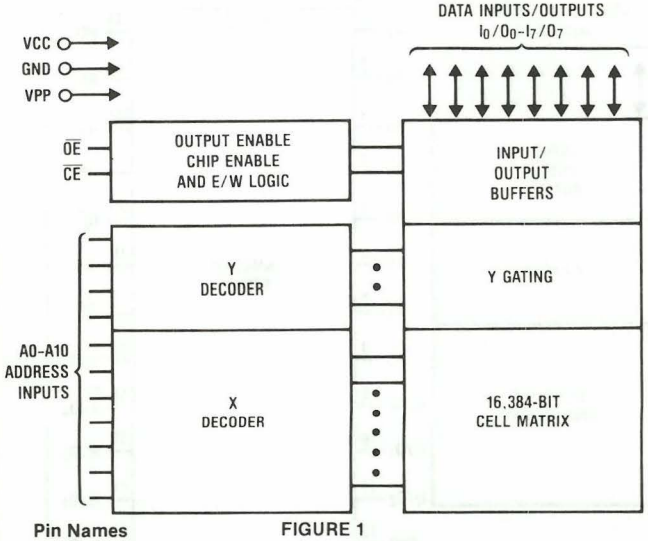
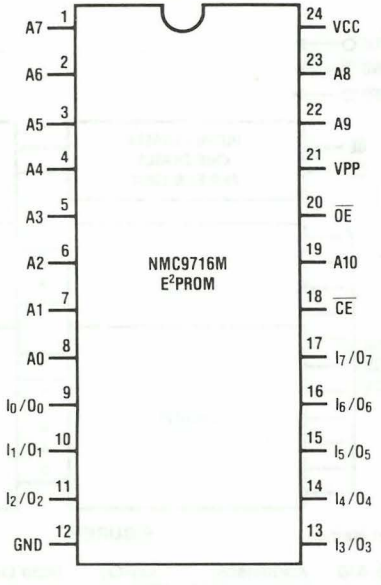


FIGURE 1

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

Dual-In-Line Package



TOP VIEW

FIGURE 2

1982 National Semiconductor Corp. WD/82

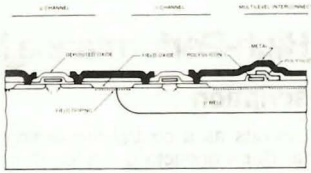
IM-B25M42/Printed in U.S.A.

Circle DATA UPDATE No. 112267

National Semiconductor

December 1981

NS80C48/80C35 P²CMOS™ Microcomputer/Microprocessor Family



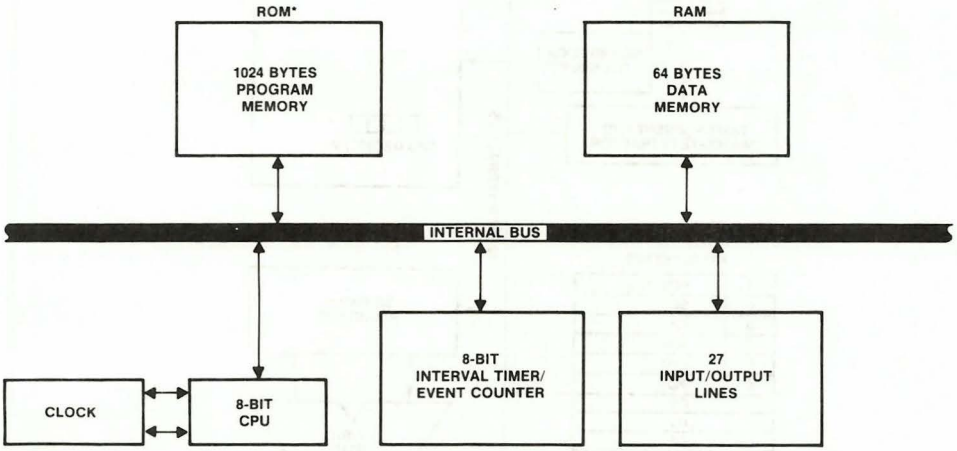
General Description

The NS80C48 is a parallel 8-bit microcomputer contained in a standard 40-pin, dual-in-line package. The device is fabricated using P²CMOS silicon gate technology. This technology provides the system designer with devices that equal the speed performance levels of comparable NMOS products, combined with low-power advantages of CMOS. The NS80C48 is a stand-alone microcomputer designed for efficient controller applications. It executes powerful bit manipulative instructions and BCD as well as binary arithmetic. The NS80C48 contains on-chip oscillator and clock circuits, 1K x 8 ROM program memory, 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit Timer/Counter. Also, it is pin and instruction compatible with the XMOS™ INS8048.

Features

- 8-Bit CPU, RAM, ROM, I/O in a Single Package
- 2.5 μsec Cycle Time, 6MHz Oscillator
- Low Power
- Very Low Stand-by Power
- Expandable Memory and I/O
- Single-Level Interrupt
- Efficient Instructions
- Instruction Compatible to INS8048
- Pin Compatible to INS8048

NS80C48/NS80C35 Block Diagram



*Not Applicable to INS80C35

31-1

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In-H/B30M121/Printed in U.S.A.

Circle DATA UPDATE No. 112362

National Semiconductor

Preliminary
April 1982

NS16032 High-Performance Microprocessor

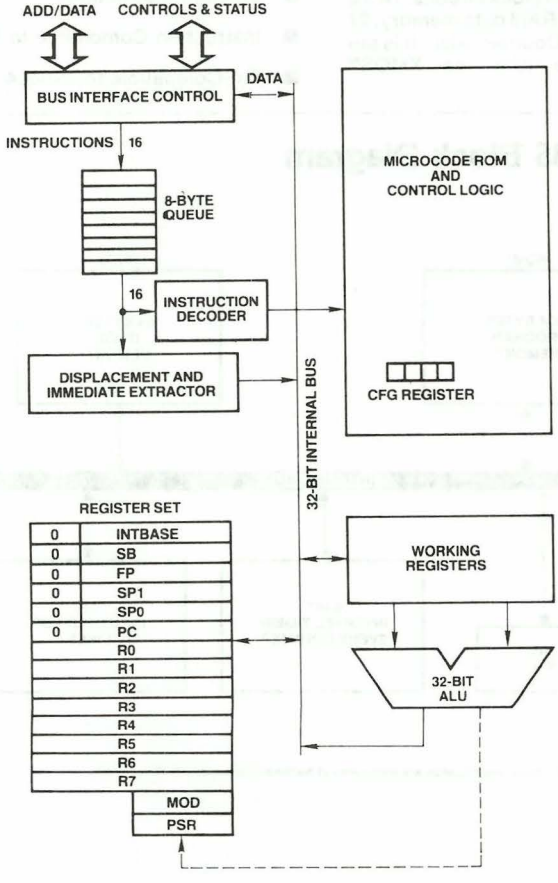
General Description

The NS16032 functions as a central processing unit (CPU) in National Semiconductor's NS16000 microcomputer family. It has been designed to optimally support microprocessor users who need the ability to use a large addressing space for large programs and/or large data structures. Because large programs must realistically be generated and maintained in high-level languages, the NS16000 architecture provides for very efficient compilation while remaining easy to program at the assembler level for optimizations. Full Virtual Memory capability is provided in conjunction with the NS16082 Memory Management Unit (MMU). High-performance Floating-Point instructions are provided with the NS16081 Floating-Point Unit (FPU).

Features

- 32-Bit Architecture and Implementation
- 16 MByte Uniform Addressing Space
- Powerful Instruction Set
  - General Two-Address Capability
  - Very High Degree of Symmetry
  - Addressing Modes Optimized for High-Level Language References
  - Expansion via Slave Processors or Traps
- High-Speed XMOS Technology
- Single 5V Supply
- 48-Pin Dual In-Line Package

NS16032 CPU Block Diagram



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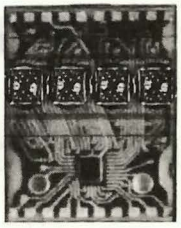
Circle DATA UPDATE No. 112350

National Semiconductor

April 1982

NSM1416 4-Digit, 16-Segment, Alphanumeric Integrated Display with Memory/Decoder/Driver



General Description

The NSM1416 is a 4-digit, alphanumeric display module with a 16-segment font and an on-board CMOS integrated circuit driver.

The four GaAsP 16-segment monolithic LEDs are magnified by an immersion bubble lens system. The driver chip is manufactured using standard complementary MOS technology. It includes memory to store four 7-bit ASCII words corresponding to the four digits, an ASCII to 16-segment alphanumeric ROM decoder, and multiplexing and drive circuitry to drive the four 16-segment monolithic digits. Inputs are TTL compatible, as is the power supply requirement. Data entry is microprocessor bus compatible with no interface circuitry required. The internal memory can be written asynchronously through the 7-bit data bus (D0–D6) into the digit location addressed by the 2-bit address bus (A0–A1).

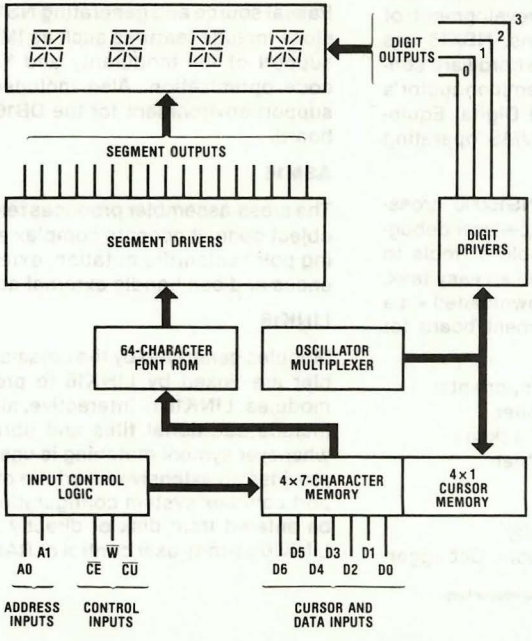
The package is extremely rugged, featuring total plastic encapsulation and sturdy pins on standard 0.1″ centers. Multiple device systems can be easily constructed by connecting data lines in parallel to the data bus. Similarly, address lines are connected in parallel to the address bus. Individual $\overline{CE}$ lines are used to select the desired 4-digit group in small (four displays or less) systems. For larger systems, a 1 of N decoder may be used to select the desired 4-digit group through the corresponding $\overline{CE}$ input. The inputs to the 1 of N decoder then become address lines $A_2, A_3 \ldots A_n$. The outputs of the decoder go to the $\overline{CE}$ inputs.

The cursor function causes all 16 segments of a digit to light, without disturbing the contents of ASCII memory corresponding to that digit. When the cursor is removed, the character displayed previous to the cursor reappears at that digit location.

Features

- End stackable for displays of many digits
- Microprocessor bus compatible
- Inputs and power supply TTL compatible (5V)
- Magnified to 0.160″
- 64-character ASCII format
- On-board memory, decoder, multiplexer and drivers
- Rugged package is totally plastic encapsulated
- Independent and asynchronous digit access
- Independent cursor function
- Ultra-fast access time, 300ns

Block Diagram



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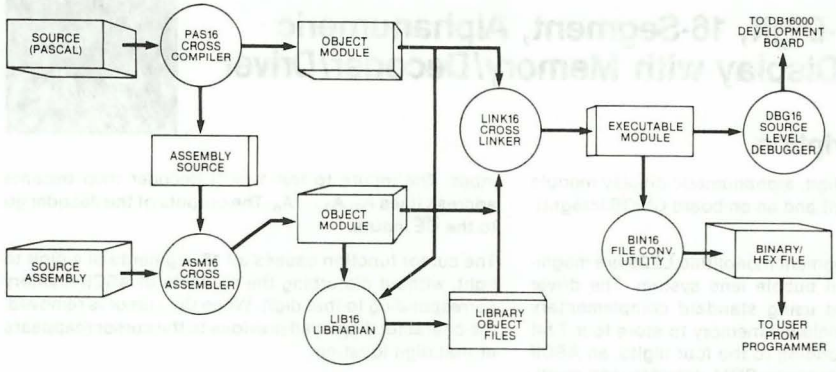
Circle DATA UPDATE No. 113220

NSM1416 4-Digit, 16-Segment, Alphanumeric Integrated Display with Memory/Decoder/Driver

National Semiconductor

July 1982

NSX16 Cross Software Package



NSX16 Cross Software Package

- **Runs under STARPLEX II™ operating system and DEC® VAX/VMS operating system**
- **Compatible with ANSI standard Pascal**
- **Supports NS16081 floating point unit**
- **Pascal run-time support environment for DB16000 development board**
- **Pascal compiler produces NS16000 code directly**
- **High-level symbolic debugger allows debug at source level**

Product Overview

NSX16 is a comprehensive software development package that includes all the components necessary to produce NS16000 native code. Intended as a support package to facilitate the development of software for NS16000-based systems, NSX16 has been designed to run initially on two hardware configurations. These are National Semiconductor's STARPLEX II operating system and Digital Equipment's VAX11 series running the VMS operating system.

Consisting of a Pascal compiler, NS16000 cross-assembler, linker, librarian, and source-level debugger, NSX16 provides the full ensemble of tools to make the generation of NS16000 code an easy task. Code thus developed may then be downloaded via a serial port to the DB16000 development board for execution and debug.

NSX16 consists of the following components:

— PAS16, the Pascal Cross-Compiler
— RTS16, the Run-Time Support Package
— ASM16, NS16000 Cross-Assembler
— LINK16, the Cross Linker
— LIB16, the Librarian
— BIN16, the File Conversion Utility
— DBG16, the Source-Level Symbolic Debugger

PAS16

Designed to be compatible with the ANSI standard, with listed extensions and restrictions, the Pascal cross-compiler is capable of accepting compatible Pascal source and generating NS16000 code. Extensions include features such as IMPORT/EXPORT in support of full modularity and FAST variables for code optimization. Also included is the run-time support environment for the DB16000 development board.

ASM16

The cross-assembler produces relocatable NS16000 object code. It accepts complex expressions, floating point scientific notation, external symbol references and can handle external address arithmetic.

LINK16

Modules generated by the cross-compiler or assembler are linked by LINK16 to produce executable modules. LINK16 is interactive, allowing the user to include additional files and libraries at link time whenever symbol matching is unsuccessful. LINK16 provides an extensive repertoire of directives to support complex system configurations. Directives can be entered from disk or directly from the console. LINK16 permits user control of RAM/ROM allocation.

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DEC is a registered trademark of Digital Equipment Corp.
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DA-B30M72/Printed in U.S.A.

Circle DATA UPDATE No. 112300

National Semiconductor

PRELIMINARY
May 1982

Programmable Array Logic Family Series 24

General Description

The PAL® Series 24 family compliments the PAL Series 20 family by providing two additional inputs and two additional outputs, allowing more complex functions in a single package. This new family is made feasible by the new 300 Mil-wide, 24-pin package.

In addition to providing more logic function per chip, 24 pins allows for many natural functions which were previously unavailable in 20-pin packages. Examples include:

- 8-bit parallel-in parallel-out counters
- 8-bit parallel-in parallel-out shift registers
- 16-Line-to-1-Line Multiplexers
- Dual 8-Line-to-1-Line Multiplexers
- Quad 4-Line-to-1-Line Multiplexers

These natural functions provide twice the density of traditional 16-pin packages.

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production. This often simplifies not only the PC board layout, but also the board itself.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

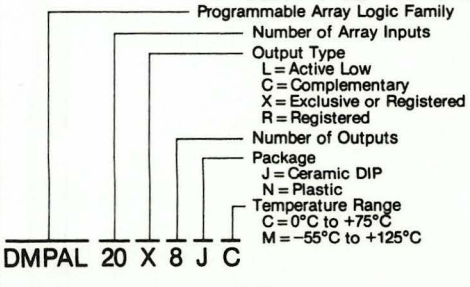
The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality cards and socket adapters. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

PAL is a registered trademark of and used under license with Monolithic Memories, Inc.

Features

- Programmable replacement for conventional TTL logic.
- Reduces IC inventories substantially and simplifies their control.
- Reduces chip count by 5 to 1, typically.
- Expedites and simplifies prototyping and board layout.
- Saves space with 300 Mil-wide, 24-pin DIP packages.
- Programmed on standard PROM programmers.
- Programmable three-state outputs.
- Last fuse reduces possibility of copying by competitors.

Ordering Information



Part Number	Description
PAL12L10	DECA 12 Input AND-OR-INVERT Gate Array
PAL14L8	OCTAL 14 Input AND-OR-INVERT Gate Array
PAL16L6	HEX 16 Input AND-OR-INVERT Gate Array
PAL18L4	QUAD 18 Input AND-OR-INVERT Gate Array
PAL20L10	DECA 20 Input AND-OR-Invert Gate Array
PAL20X10	DECA 20 Input Registered AND-OR-XOR Gate Array
PAL20X8	OCTAL 20 Input Registered AND-OR-XOR Gate Array
PAL20X4	QUAD 20 Input Registered AND-OR-XOR Gate Array

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DA-B25M52/Printed in U.S.A.

Circle DATA UPDATE No. 114402

National Semiconductor

PRELIMINARY
July 1982

SCX Gate-Array Design Automation System

Product Overview

The objectives of National's Gate Array Design Automation System are

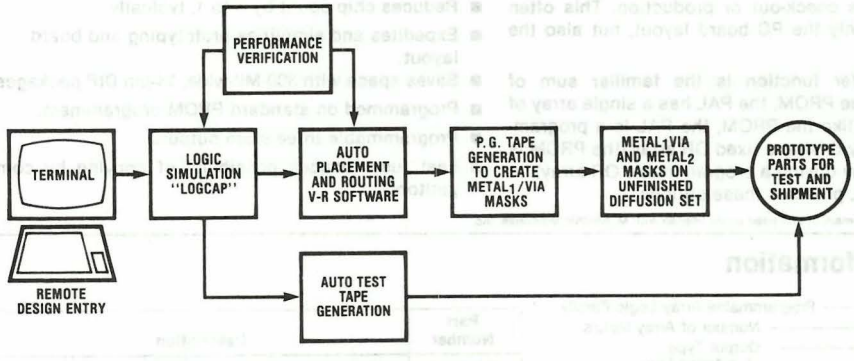
- To achieve automated layouts of complex logic circuits by using "macrocells" from the reference library with 2-layer metal interconnects.
- Automatic cell placement and high-yield interconnect routing.
- To provide automatic layout and logic verification for error-free designs.

TRI-STATE is a registered trademark of National Semiconductor Corporation.

Features

- Graphics entry
- Logic simulation
- Automatic placement
- Automatic routing
- Performance verification
- P.G. tape compatibility

Development System for Gate-Arrays Diagram


PERFORMANCE VERIFICATION
TERMINAL
LOGIC SIMULATION "LOGCAP"
AUTO PLACEMENT AND ROUTING V-R SOFTWARE
P.G. TAPE GENERATION TO CREATE METAL1/VIA MASKS
METAL1 VIA AND METAL2 MASKS ON UNFINISHED DIFFUSION SET
PROTOTYPE PARTS FOR TEST AND SHIPMENT
REMOTE DESIGN ENTRY
AUTO TEST TAPE GENERATION

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DA-B10M72/Printed in U.S.A.

Circle DATE UPDATE No. 535018

September 1982

National Semiconductor

SCX 6324A High-Performance 2.4k CMOS Gate Array Macro Library Specifications

General Description

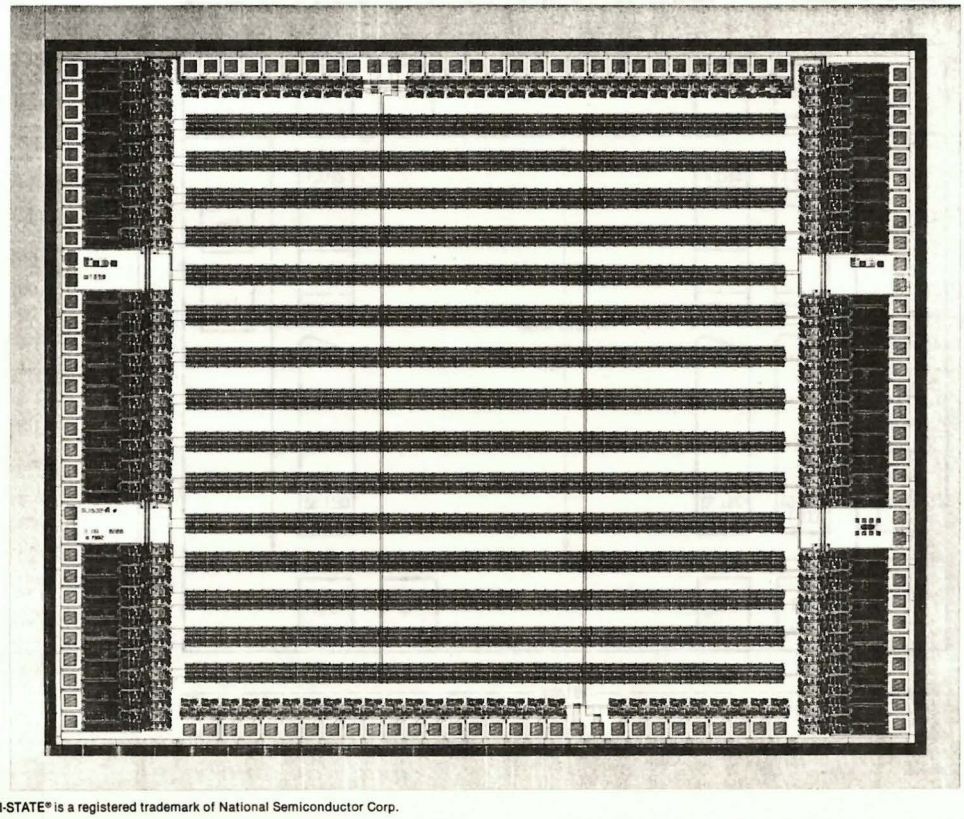
This versatile 2.4k gate array utilizes silicon-gate dual-layer metal CMOS (M^2CMOS) technology to achieve operating speeds similar to S-TTL with the inherent lower power consumption of standard CMOS integrated circuits. All outputs have the ability to drive 10 LSTTL loads. All inputs have high noise immunity and are protected from damage due to static discharge.

To enhance user applications, the device is offered in three attractive 124-pin package options. Smaller pin count packages are available upon request.

Features

- 2.4k gates
- 2.0ns internal t_{PD}
- CMOS power dissipation
- "LS" drive capability
- Full design automation support
  - —80% utilization
  - —100% auto place and route
- 124 pins maximum
  - —55 inputs
  - —56 I/Os
  - —6 V_{DD}
  - —6 V_{SS}
  - —1 test

SCX 6324A Topology



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DA-B25M92/Printed in U.S.A.

Circle DATA UPDATE No. 113588

National Semiconductor

PRELIMINARY
April 1982

SLX6324 - High Speed 2.4k CMOS Gate Array

General Description

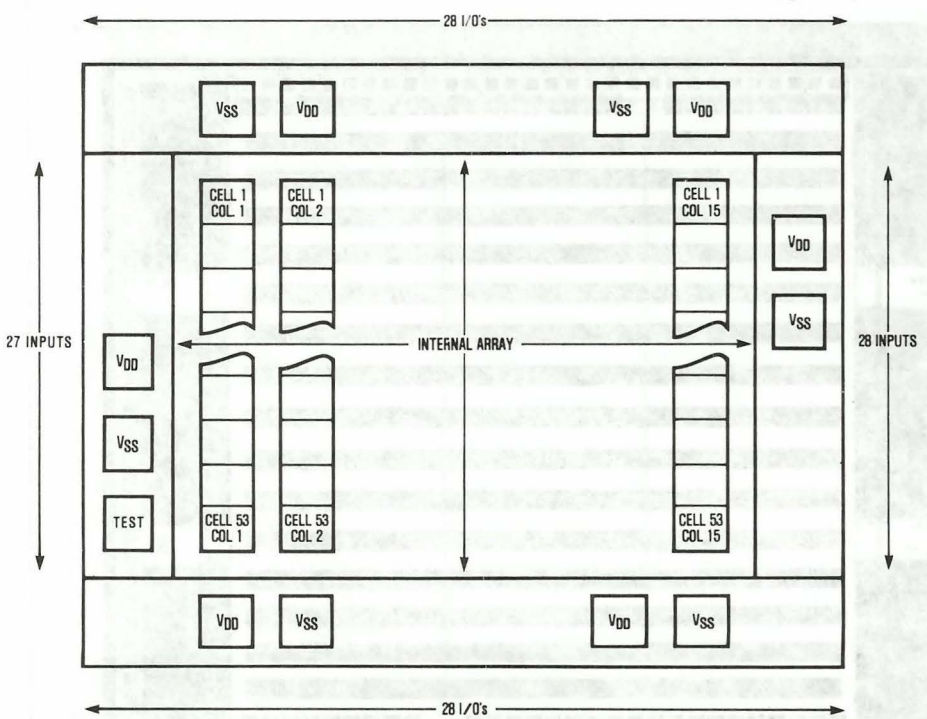
This versatile 2.4k gate array utilizes silicon gate dual layer metal CMOS (M²CMOS) technology to achieve operating speeds similar to LS-TTL with the inherent lower power consumption of standard CMOS integrated circuits. All outputs have the ability to drive 10LS-TTL loads. All inputs have high noise immunity and are protected from damage due to static discharge.

To enhance user applications, the device is offered in three attractive 124-pin package options. Smaller pin count packages are available upon request.

Features

- 2.4k Gates
- 2.0ns Internal t_{pd}
- CMOS Power Dissipation
- "LS" Drive Capability
- Full Design Automation Support
  - — 80% Utilization
  - — 100% Auto Place and Route

Topological Diagram



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Circle DATA UPDATE No. 113590

National Semiconductor

PRELIMINARY
May 1982

TP3051, TP3056 Monolithic Parallel Data Interface CMOS CODEC/Filter Family

TP3051, TP3056 Monolithic Parallel Data Interface CMOS CODEC/Filter Family

General Description

The TP3051, TP3056 family consists of a μ-law and A-law monolithic PCM CODEC/filter set utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a parallel I/O data bus interface. The devices are fabricated on National's advanced double-poly CMOS process (P^2CMOS).

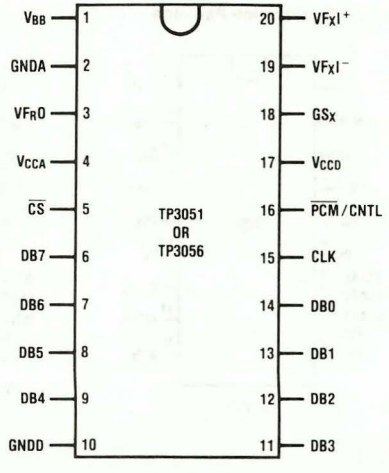
The transmit section consists of an input gain adjust amplifier, an active RC pre-filter, and a switched-capacitor bandpass filter that rejects signals below 200 Hz and above 3400 Hz. A compressing coder samples the filtered signal and encodes it in the μ-255 law or A-law PCM format. Auto-zero circuitry is included on-chip. The receive section consists of an expanding decoder which reconstructs the analog signal from the compressed μ-law or A-law code, and a low pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz. The receive output is a single-ended power amplifier capable of driving low impedance loads. The TP3051 μ-law and TP3056 A-law devices are pin compatible parallel interface CODEC/filters for bus-oriented systems. They are ideally suited for use with the TP3100 family of digital line interface controllers (DLIC) in switching system applications. The DLIC communicates with the main switch controller via integrated data, signaling and control channels, and provides local time-slot and space switching capability for up to 32 TP3051 or TP3056 CODECs.

Features

- Complete CODEC and filtering system including:
  - -Transmit high pass and low pass filtering
  - -Receive low pass filter with sin x/x correction
  - -Receive power amplifier
  - -Active RC noise filters
  - -μ-255 law COder and DECoder—TP3051
  - -A-law COder and DECoder—TP3056
  - -Internal precision voltage reference
  - -Internal auto-zero circuitry
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- High speed TRI-STATE® data bus
- 2 loopback test modes

Connection Diagram

Dual-In-Line Package



TOP VIEW

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IM-B25M52/Printed in U.S.A.

Circle DATA UPDATE No. 113974

National Semiconductor

March 1982
PRELIMINARY

TP3052, TP3053, TP3054, TP3057 Monolithic Serial Interface CMOS CODEC/FILTER Family

General Description

The TP3052, TP3053, TP3054, TP3057 family consists of μ-law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (P^2CMOS^{TM}).

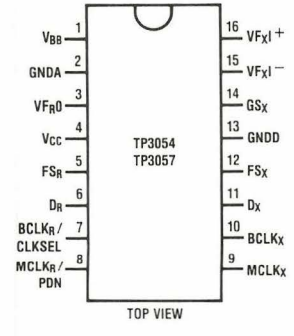
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded μ-law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks, which are synchronous with the master clocks but may vary from 64 kHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

- Complete CODEC and filtering system (COMBO) including:
  - -Transmit high-pass and low-pass filtering
  - -Receive low-pass filter with sin x/x correction
  - -Active RC noise filters
  - -μ-law or A-law compatible COder and DECoder
  - -Internal precision voltage reference
  - -Serial I/O interface
  - -Internal auto-zero circuitry
- μ-law with signaling, TP3020 timing—TP3052
- μ-law with signaling, TP5116A family timing—TP3053
- μ-law without signaling, 16-pin—TP3054
- A-law, 16-pin—TP3057
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density

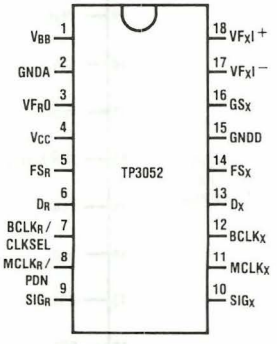
Connection Diagrams

Dual-In-Line Package



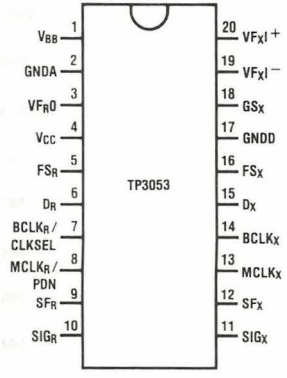
TOP VIEW

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



P^2CMOS^{TM} is a trademark of National Semiconductor Corp.

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Circle DATA UPDATE No. 113975

TP3052, TP3053, TP3054, TP3057 Monolithic Serial Interface CMOS CODEC/FILTER Family

National Semiconductor

PRELIMINARY
June 1982

TP3310, TP3311, TP3320, TP3321 Monolithic 1200/75 Bit/s FSK MODEM Family

TP3310, TP3311, TP3320, TP3321 Monolithic 1200/75 Bit/s FSK MODEM Family

General Description

The TP3320 and TP3321 are general purpose monolithic FSK (frequency shift-keyed) MODEMs implemented with National's advanced double-poly CMOS process (P^2CMOS^{TM}). They are capable of generating and receiving frequency modulated signals at data rates from 0 to 600 bit/s or from 0 to 1200 bit/s on voice-grade telephone lines. The operating mode can be half-duplex with a backward channel on two-wire lines or full-duplex on four-wire lines. The TP3320 and TP3321 are offered in a 20-pin package and are capable of operating according to three standards:

—CCITT V23 at 1200 bit/s, with backward channel at 75 bit/s.
—CCITT V23 at 600 bit/s, with backward channel at 75 bit/s.
—BELL 202 at 1200 bit/s, with backward channel at 5 bit/s.

The standard and the operating mode are pin selectable.

In half-duplex mode the forward and reverse channels can be used simultaneously while still maintaining excellent distortion and error-rate performance.

All filtering functions required for frequency generation, out-of-band noise rejection and demodulation are performed by on-chip switched capacitor filters.

All internal frequencies are generated from an inexpensive 3.579545 MHz TV color-burst crystal reference. The buffered master clock is made available for external use on one of the pins.

Two baud rate clocks CLK_X and CLK_R are also provided by the MODEM to synchronize the transmit and the receive section of a UART. The frequency of each clock is 16 times the baud rate for the associated direction (75×16 Hz, 600×16 Hz or 1200×16 Hz, depending on the operating mode).

The handshaking protocol of the TP3320 and TP3321 with the local data terminal is RS232C compatible. The self-test feature allows the user to locally test the forward and the reverse channel of the MODEM.

A power-down mode is provided to reduce the power consumption to less than 2 mW when the MODEM is inactive.

The TP3310 and TP3311 are 16-pin versions of the TP3320 optimized for VIEWDATA terminals and for applications where low cost and board area are important considerations. They are still complete half-duplex or full-duplex MODEMs; but they only operate according to CCITT standard V23 with a 1200 bit/s main channel and a 75 bit/s backward channel.

To realize a low cost data terminal, the MODEM can be interfaced with a UART and a microprocessor as shown in *Figure 1*. The standard and the operating mode are controlled by the microprocessor. No external baud rate generator is needed.

Features

- ± 5V operation
- Low operating power dissipation: 75 mW (typical)
- Low standby power dissipation: 2 mW (typical)
- On-chip switched capacitor transmit and receive filters
- Uses inexpensive 3.579545 MHz television color-burst crystal
- BELL 202(s) compatible
  - 0–1200 bit/s with 5 bit/s reverse channel
  - 900 Hz soft carrier turn-off tone
- CCITT V23 compatible
  - 0–1200 bit/s with 75 bit/s reverse channel
  - 0–600 bit/s with 75 bit/s reverse channel
- Half-duplex operation on two-wire lines
- Full-duplex 1200 bit/s operation on four-wire lines
- Optimized UART interface
- Loopback test mode
- RS232C-type handshake signals

Applications

- Built-in medium speed MODEMs
- Stand-alone MODEMs
- VIDEOTEX or VIEWDATA terminals
- Remote data collection
- Point of sale terminals
- Credit verification systems
- Tape recorder interface
- Electronic mail

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Circle DATA UPDATE No. 113990

National Semiconductor

PRELIMINARY
July 1982

TP5087/TP5087A, TP5092/TP5092A, TP5094/TP5094A DTMF (TOUCH-TONE®) Generators

General Description

The TP5087, TP5092 and TP5094 are low threshold voltage, field-implanted, metal gate CMOS integrated circuits. The devices interface directly to a standard telephone keypad and generate all dual tone multi-frequency pairs required in tone-dialing systems. The tone synthesizers are locked to an on-chip reference oscillator using an inexpensive 3.579545 MHz crystal for high tone accuracy. The crystal and an output load resistor are the only external components required for tone generation. A MUTE OUT logic signal, which changes state when any key is depressed, is also provided.

Features

- 2.5V–10V operation when generating tones (TP5087A, TP5092A, TP5094A)
- 2V operation of keyscan and MUTE logic
- Powered directly from telephone line
- Interfaces with standard single-contact or 2-of-8 telephone keypad
- Static sensing of key closures
- On-chip 3.579545 MHz crystal-controlled oscillator
- On-chip regulation of tone amplitudes
- High group and low group tones generated and mixed internally
- High group pre-emphasis
- Low harmonic distortion
- Open emitter-follower low-impedance output
- $\overline{\text{SINGLE TONE INHIBIT}}$ pin

Block Diagram

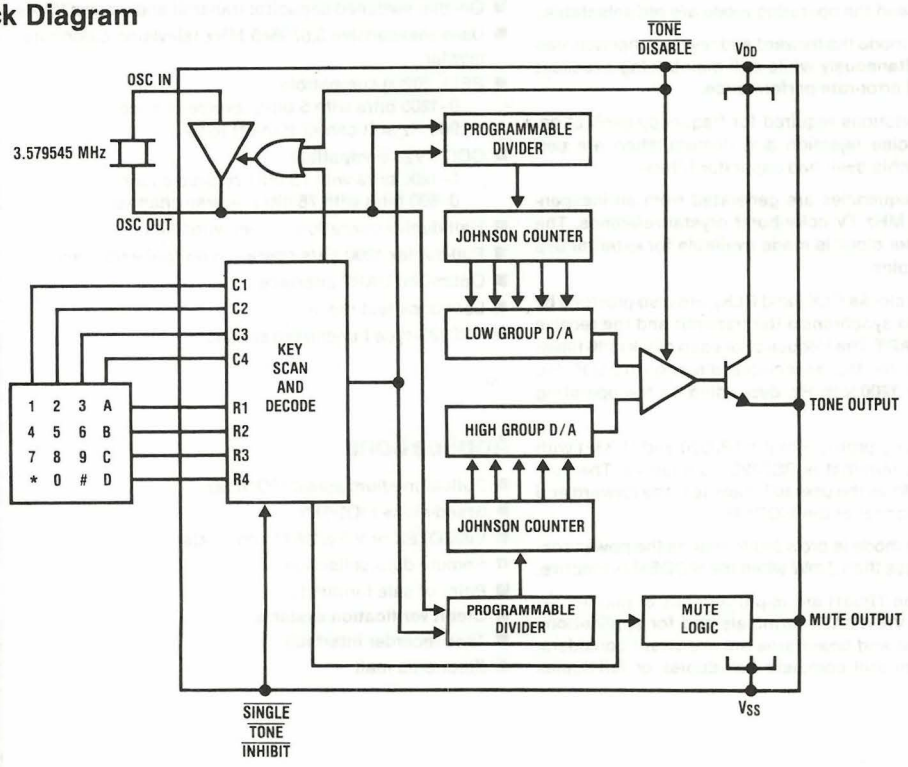

FIGURE 1. TP5087 Family

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Circle DATA UPDATE No. 113995

National Semiconductor

May 1982

Z80®EMULATOR PACKAGE

- **Real-time emulation of Z80, Z80A® and Z80B® microprocessors**
- **Supports two modes of operation**
  - Program development
  - Single processor emulation
- **Plugs directly into any STARPLEX™/ STARPLEX II™ development system**
- **Includes target board, cable pod with cables and complete software**

Product Overview

National's Z80 Emulator Package gives the designer of Z80 based systems the kind of sophisticated tool required for efficient microcomputer development. The Z80 Emulator Package, in conjunction with the Integral ISE™ Package and a STARPLEX/STARPLEX II Development System, provides capabilities that up to now have not been available in this type of instrument.

National's Integral ISE Package is installed directly into any STARPLEX/STARPLEX II Development System. This package consists of two logic boards (TRACE logic and MAPPED MEMORY). These two logic boards provide the user with 32 K bytes of real-time map memory and all the necessary logic for break-points, tracing and memory mapping. These resources are available for the emulation of any processor since the individual emulation packages are the only components dedicated to particular processors. This approach simplifies changing processors since the user needn't learn a new ISE™ language each time he changes emulation packages.

The Z80 Emulator Package provides the physical and electrical interface between the Integral ISE package, the STARPLEX Development System and a Z80 based system undergoing development. When installed in a STARPLEX Development System, it connects to the user's system via the cable pod and a 40-pin plug to the system under development. In this configuration, the entire system supports two modes of operation. These modes are program development and single processor emulation.

The program development mode permits the user to develop and debug his software even though he has no prototype hardware available. The emulator package provides the clocks and memory necessary for this task. During emulation of a single processor, the user's hardware provides the actual clock signal, thus forcing the entire Integral ISE system to operate at the actual clock rate of the user's system.

Z80 (6 MHz) Emulator Package Option

An optional 6 MHz Z80 Emulator Package is available for first time users who want to do real-time emulation of the Z80B microprocessor. Included in this package are: target board, lightweight plastic cable pod, cables, software for ISE Host Driver, Z80 Display Change software of mnemonic assembly and disassembly, trace board, high-speed (55 ns) 32 K bytes mappable memory board and TTL status pod. (SPM-A20 also includes Z80 (NSC800™) Cross-Assembler Software.)

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Circle DATA UPDATE No. 611560

THE DATA BOOKSHELF: TOOLS FOR THE DESIGN ENGINEER

National Semiconductor's Data Bookshelf is a compendium of information about a product line unmatched in its breadth in the industry. The fifteen independent volumes that comprise the Bookshelf—about 8000 pages—describe in excess of 8100 solid-state devices; devices that span the entire spectrum of semiconductor processes, and that range from the simplest of discrete transistors to microprocessors—those most-sophisticated marvels of modern integrated-circuit technology.

Active and passive devices and circuits; hybrid and monolithic structures; discrete and integrated components ... complete electrical and mechanical specifications; charts, graphs, and tables; test circuits and waveforms; design and application information...whatever you need, you'll find it in the designer's ultimate reference source—National Semiconductor's Data Bookshelf.

ADVANCED BIPOLAR LOGIC DATABOOK

This is the Advanced Bipolar Logic Databook from National Semiconductor. The book contains information on the Advanced Schottky family, as well as the most up-to-date information available from National on the Advanced Low Power Schottky family.

Both of these advanced logic families are in their early production phases and will be continually expanded in future National Databook publications.

Contact your National Semiconductor Representative for more information concerning these next generation logic families or any of the other extensive logic families.

Page Count: 214 Price: $5.00 Year: 1982

CMOS DATA BOOK

This databook contains information on National Semiconductor's standard SSI/MSI CMOS products. This includes the popular 54C74C series logic family, which is pin for pin, function for function equivalent to the 7400 family of TTL devices. All device outputs are LPTTL compatible, capable of sinking more than 360μA ($\approx$ 1 LSTTL load). The AC parameters are specified with a 50pF capacitive load.

In addition, this book describes National Semiconductor's extensive line of CD40XXB and CD45XXB series devices. These parts meet the standard JEDEC "B-Series" specifications.

Special Function, LSI, A/D Converters and Memory device specifications contained herein offer the designer unique high-density low-power system solutions. All devices are compatible with 54C/74C series and CD4XXB series products.

Page Count: 842 Price: $6.00 Year 1981

COPS MICROCONTROLLERS DATABOOK

The COPS Microcontrollers Databook offers the most current information available from National Semiconductor on the COPS microcontroller family. Included in this publication are sections on: single-chip, ROMless and piggyback microcontrollers, standard controllers, MICROWIRE peripherals, EPROMs and support circuits, and development systems and user's manuals, as well as the applications for these products.

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Page Count: 834 Price: $6.00 Year: 1982

48-SERIES MICROCOMPUTER HANDBOOK

This handbook contains detailed design-related information pertaining to the National Semiconductor 48-Series single-chip microcomputers and microprocessors.

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Page Count: 192 Price: $5.00 Year: 1980

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Page Count: 1952 Price: $12.00 Year: 1982

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Page Count: 464 Price: $6.00 Year: 1980

NSC800 MICROPROCESSOR FAMILY HANDBOOK

Contained in this manual are 224 pages of design-related information about National Semiconductor's 800-family series of high-performance-power microprocessor components.

Included are hardware functions, software operations, system support and design considerations for the NSC800 CPU, the NSC810 I/O Timer, and the NSC830 ROM I/O.

Completing this current edition are data sheets, application notes, and physical dimensions for many of the NSC800 components fabricated using the P²CMOS process.

Page Count: 224 Price: $5.00 Year: 1981

PAL™ DATABOOK

This book is intended to be a complete reference for the design of digital systems using Programmable Array Logic (PAL) devices. In addition to data sheets for all currently available devices, this book also contains extensive application notes intended to give design examples for a number of PAL devices. It also contains a step-by-step procedure for PAL design and programming, including the listing for PALASM™, which is a FORTRAN IV program that converts logic equations to PAL programming information.

Portions of this book have been reprinted with the permission of Monolithic Memories Inc., the originator of the PAL concept.

Page Count: 176 Price: $6.00 Year: 1982

RELIABILITY HANDBOOK VOLUME I

The Reliability Handbook Volume I penetrates the barrier of technical jargon and procedural ritual that has grown around the subject of semiconductor reliability, enabling the reader to arrive at a clearer understanding in the areas that bear direct concern in the application of semiconductors within the Military/Aerospace electronic systems.

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